

B1 V1 DDR4*2 Channel

Intel Gemini Lake Refresh Platform

01--COVER PAGE
02--BLOCK DIAGRAM
03--POWER BLOCK DIAGRAM
04--SYSTEM LIST
05--GLK_SOC_MEM(CHA)
06--GLK_SOC_MEM(CHB)
07--GLK_SOC_(EMMC/SPI/LPC/AUD/PMU)
08--GLK_SOC(DDI/DSI)
09--GLK_SOC(I2C/CNV/LPSS/SPI/UART)
10--GLK_SOC(PCIE/SATA/USB)
11--GLK_SOC(JTAG/GPIO)
12--GLK_SOC(PWR)
13--GLK_SOC(GND)
14--GLK_SOC(DECAP)
15--GLK_SOC(STRAP)
16--MEM_DDR4_CHA0
17--MEM_DDR4_CHA1
18--MEM_DDR4_CHB0
19--MEM_DDR4_CHB1
20--MEM_DECAPS
21--DDR4_ CHA_TERMINATIONS
22--DDR4_ CHB_TERMINATIONS
23--SYSTEM_SPI_FLASH
24--HDMI
25--EDP
26--EDP_CONN
27--EMMC
28--SSD

29--Touch Pannel&G_SENSORS&HALL
30--RTC
31--WLAN
32--USB3.0
33--EC ITE8987
34--EC ROM &THERMAL SENSOR
35--SD CARD
36--KeyBoard&TouchPad
37--IO BOARD CONN
38--TPM
39--LAN & PEN
40--Debug conn&Changer LED
41--TYPEC MULTIPLEXER
42--TYPEC CONN
43--TYPEC POWER
44--POWER DELIVERY DCIN
45--POWER DELIVERY CHARGER
46--POWER DELIVERY 3P3V
47--POWER DELIVERY 5P5V
48--PMIC RT5077_1
49--PMIC RT5077_2
50--POWER DELIVERY VDDQ
51--POWER DELIVERY LOAD SWITCH
52--POWER DELIVERY_Backlight
53--POWER DELIVERY_PEN CHARGE
54--AC POWER ON SQUENCE 1
55--DC POWER ON SQUENCE 2
56--16P_CONN & RTL8111H
57--RJ45
58--HOLE&BOSS
59--CHANGE LIST

Vinafix.com



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NB2372

Rev V1.0

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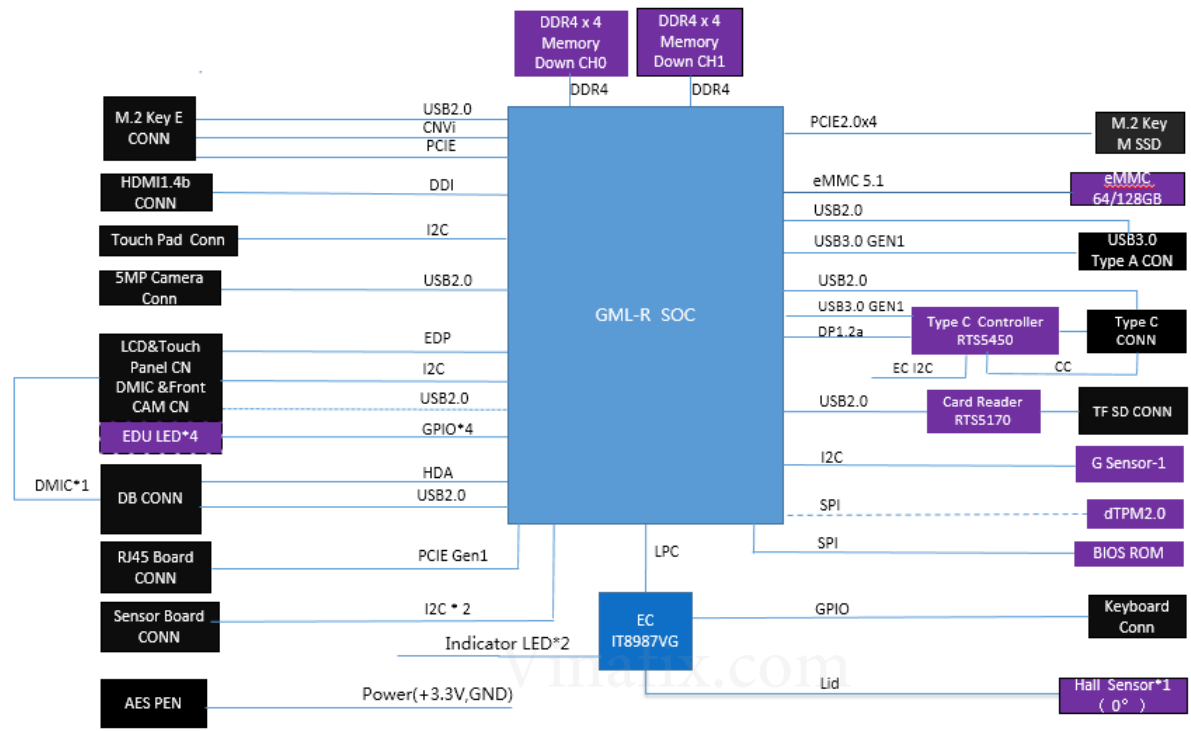
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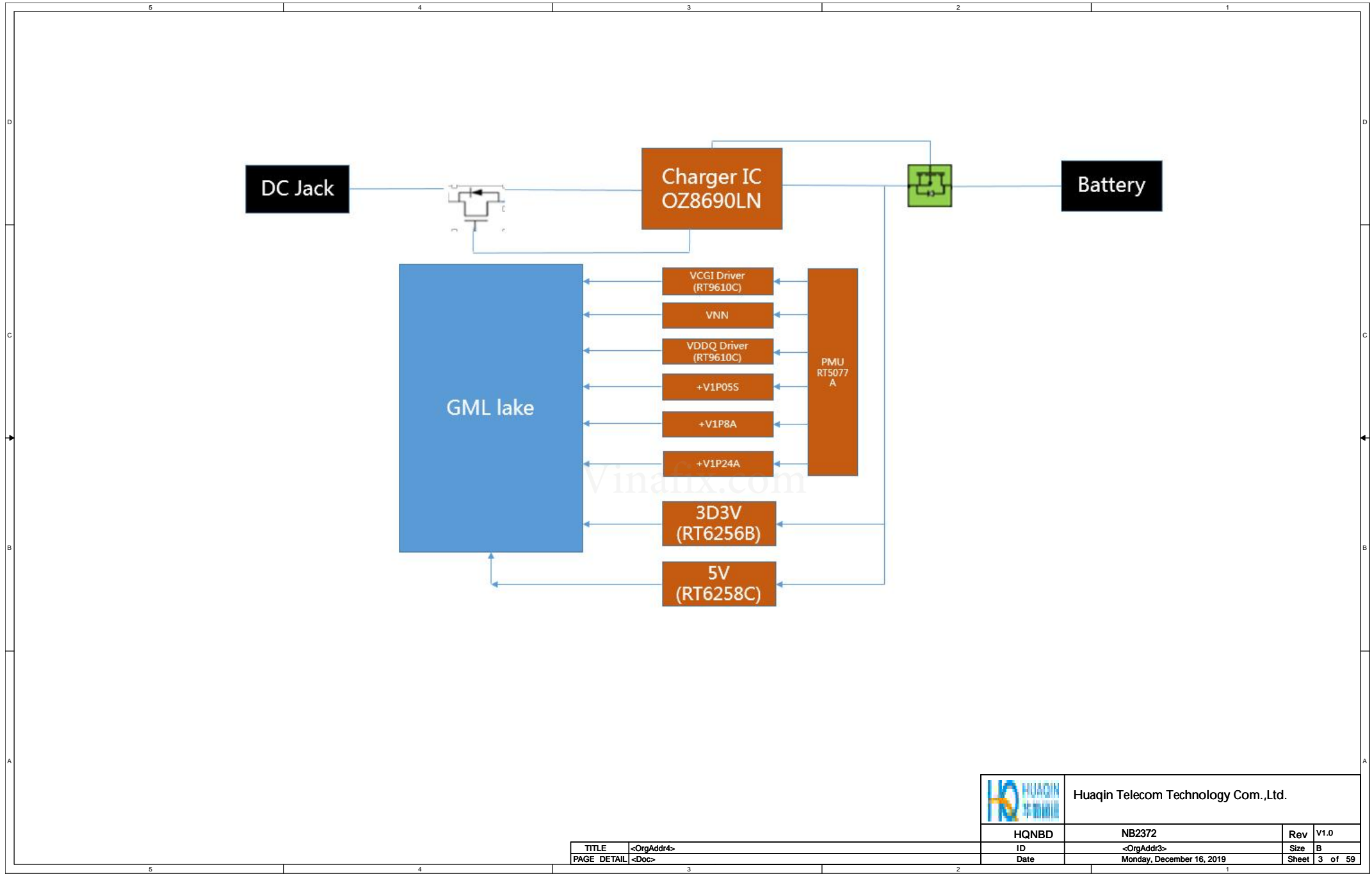
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Power States(Adapter)

Signal	SLP_S0#	SLP_S3#	SLP_S4#	+V5P0A	+V3P3A	VNN	V1P8A	V1P2A	VCGI	V1P05S	+V1P2U_VDDQ	+3P3SX	+1P8SX	+5P0SX	+V3P3SX_CWS
S0(Full On)	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON
S3(STM)	LOW	LOW	HIGH	ON	ON	OFF	ON	ON	OFF	OFF	ON	OFF	OFF	OFF	ON/OFF ¹
S4(STD)	LOW	LOW	LOW	ON	ON	OFF	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF	ON/OFF ¹
S5(SoftOff)	LOW	LOW	LOW	ON	ON	OFF	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF	ON/OFF ¹

Note1:CNVi moudle on,PCie moudle off

Power States(Battery)

Signal	SLP_S0#	SLP_S3#	SLP_S4#	+V5P0A	+V3P3A	VNN	V1P8A	V1P2A	VCGI	+V1P05S	+V1P2U_VDDQ	+3P3SX	+1P8SX	+5P0SX	+V3P3SX_CWS
S0(Full On)	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON
S3(STM)	LOW	LOW	HIGH	ON	ON	OFF	ON	ON	OFF	OFF	ON	OFF	OFF	OFF	ON/OFF ¹
S4(STD)	LOW	LOW	LOW	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON/OFF ¹
S5(SoftOff)	LOW	LOW	LOW	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON/OFF ¹

Note1:CNVi moudle on,PCie moudle off

MEM ID

MEM_ID2	MEM_ID1	MEM_ID0	
0	0	0	4x HYNIX 1GB(H5AN8G6NCJR-VKC)
0	0	1	4x Micron 1GB(MT40A512M16LY-075:E)
0	1	0	(512*16)H5AN8G6NCJR-VKC HYNIX
0	1	1	8x MT40A512M16LY-075:E MICRON
1	0	0	xxx
1	0	1	xxx

PCle Port

Port	Device
0-3	SSD
4	LAN
5	WLAN

SATA Port

Port	Device
0	SSD

USB2.0 Port

Port	Device
0	USB3.0 Type-A
1	Rear Camera
2	USB3.0 Type-A(DB)
3	USB3.0 Type-C
4	WLAN
5	Touch screen
6	Front Camera
7	SD Card

USB3.0 Port

Port	Device
0	USB3.0 Type-A
1	USB3.0 Type-C
5	USB3.0 Type-A(DB)

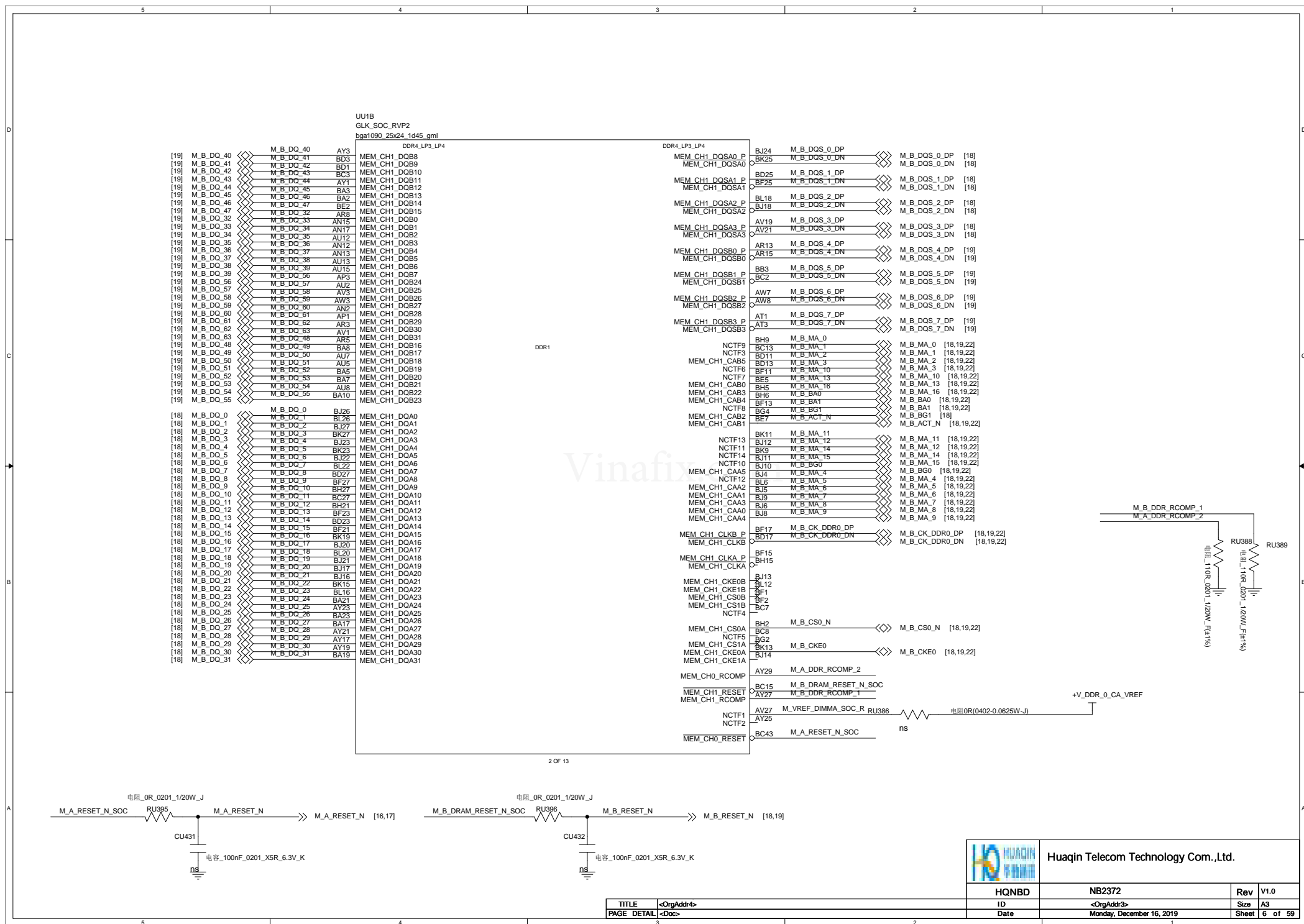
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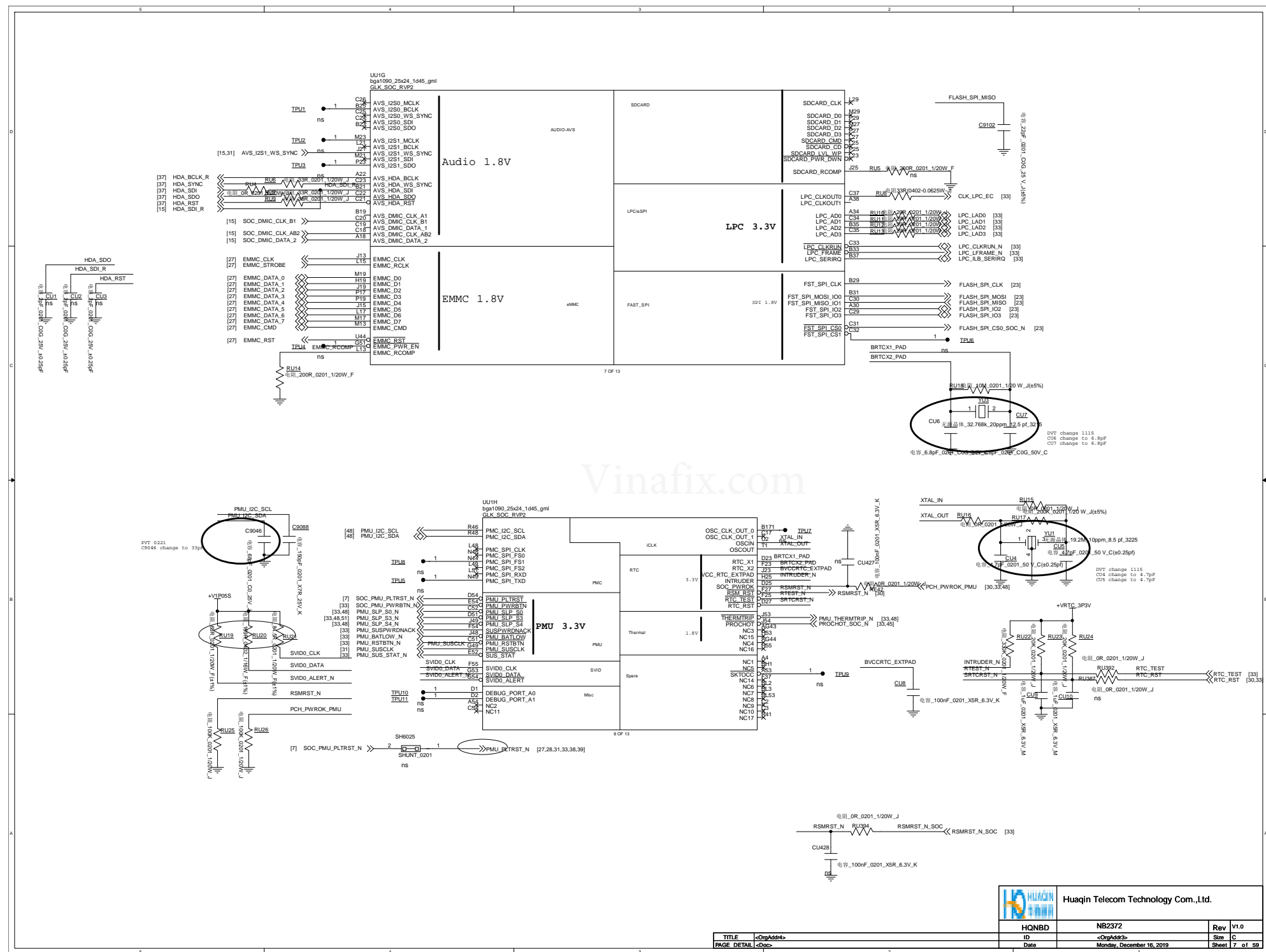
			HW_ID6	HW_ID5	HW_ID2	HW_ID1	HW_ID0
NB2372	DVT	Clamshell(180°)	X	X	1	1	0
NB2372	DVT	Convertible 860°	X	X	1	1	1

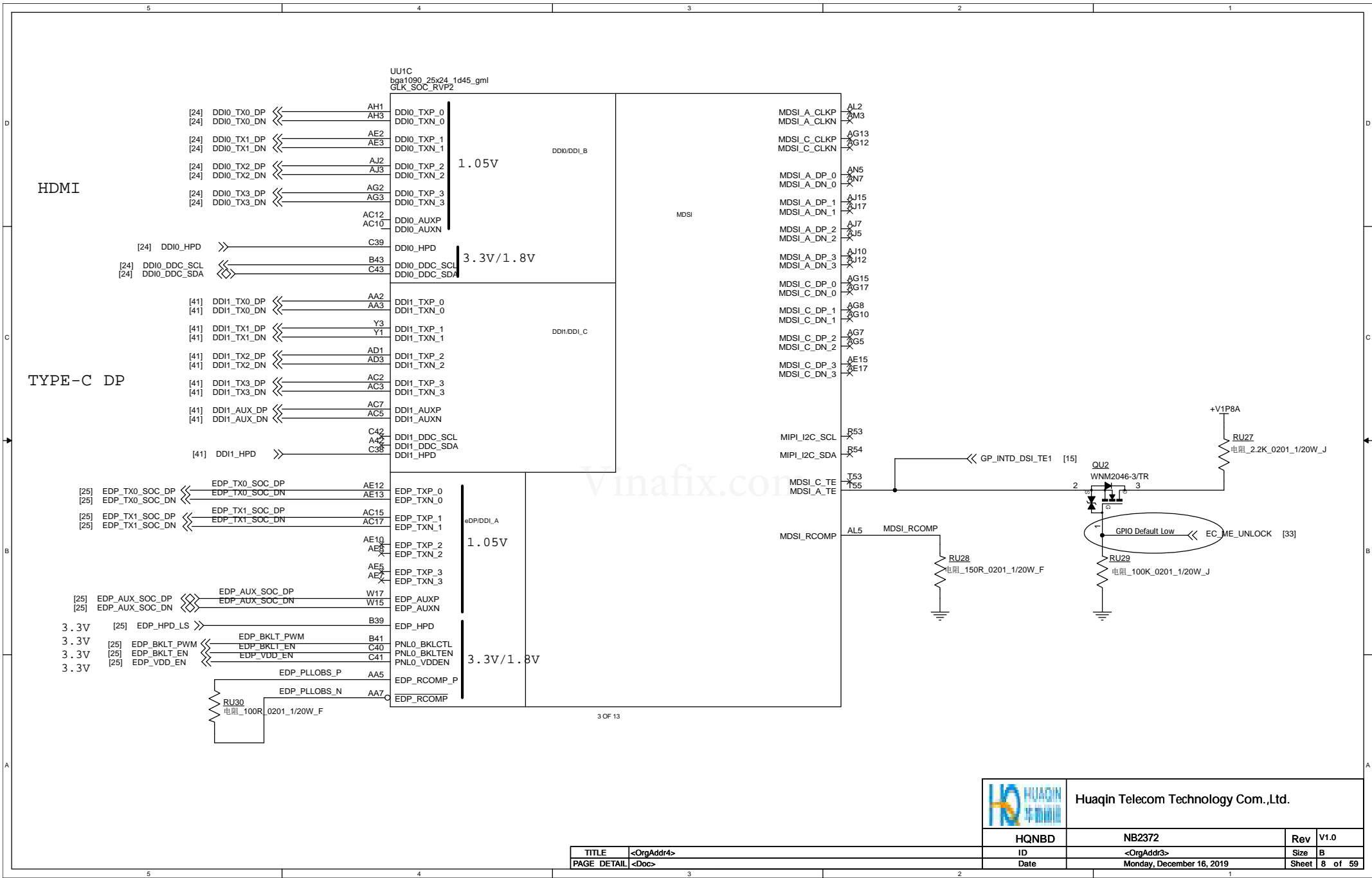



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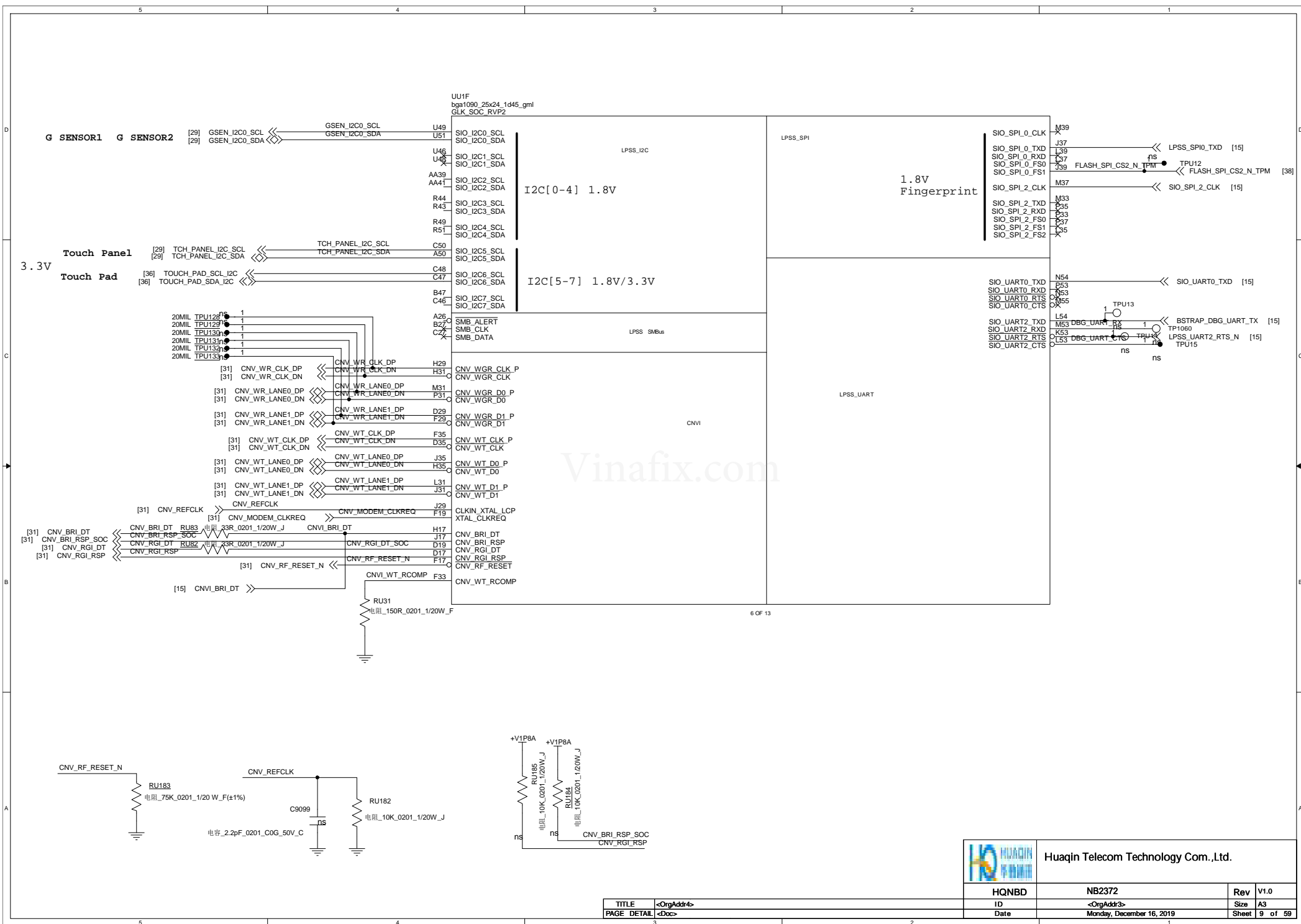
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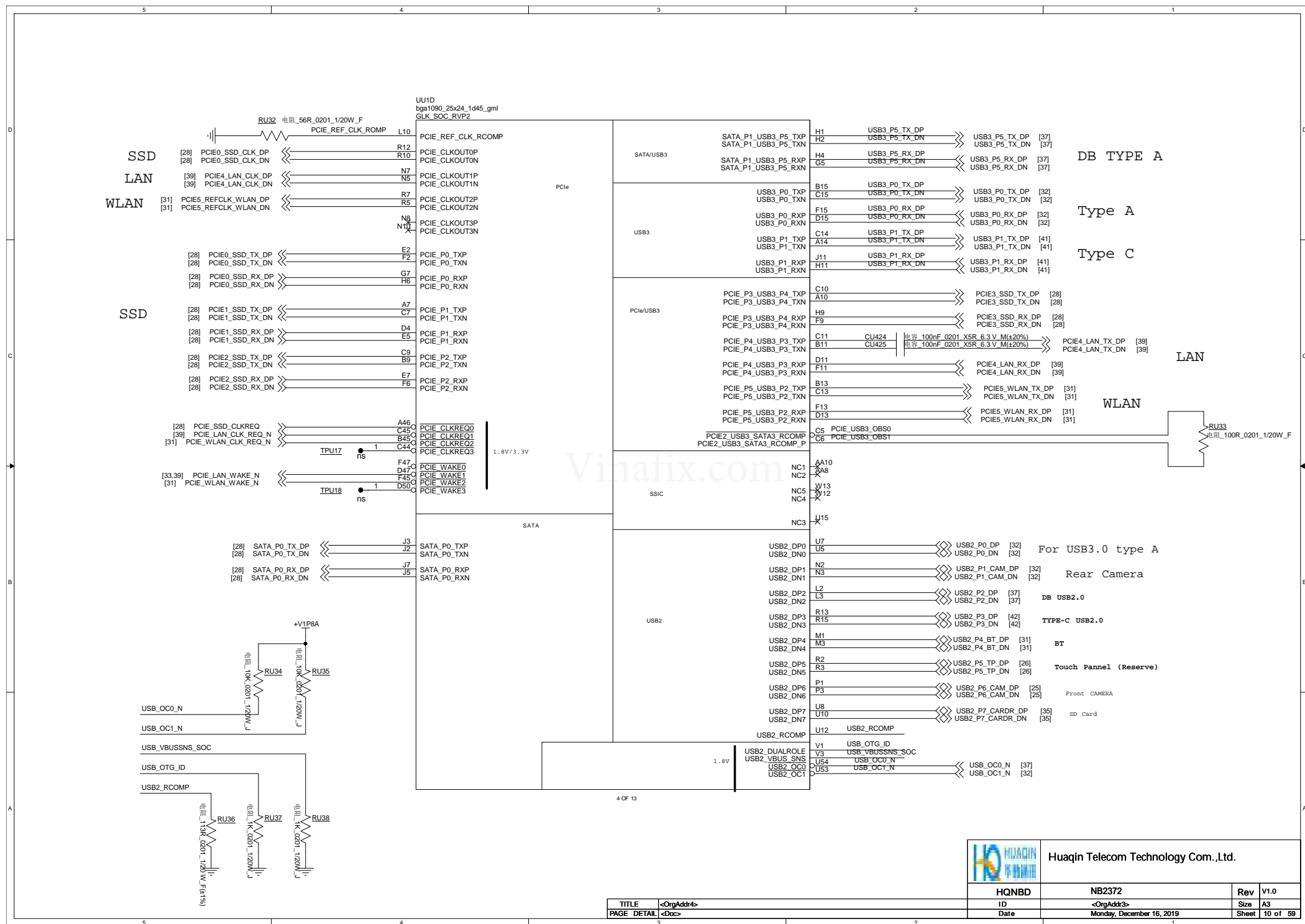






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GLK SOC RVP2

TPU19 1 AH53 JTAGX
TPU20 1 AM53 JTAG_TCK
TPU21 1 AJ54 JTAG_TDI
TPU22 1 AL53 JTAG_TDO
TPU23 1 AK53 JTAG_TMS
TPU24 1 ns JTAG_TRST
ns
TPU26 1 AH55 JTAG_PRDY
TPU27 1 AJ53 JTAG_PREQ
ns
ns

JTAG

ITP

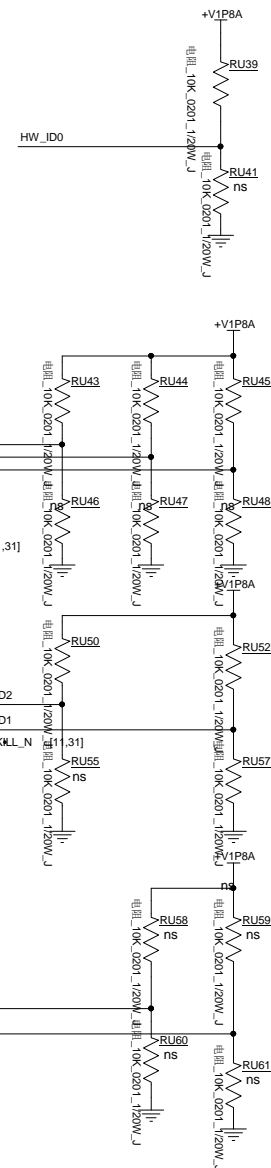
GPIO

1.8V

1.8V/3.3V

1.8V

GPIO_8 AG53
GPIO_9 AG54 << PMU_AC_PRESENT [33]
GPIO_10 AE53
GPIO_11 AD55
GPIO_12 AD53
GPIO_13 AC54
GPIO_14 AC53
GPIO_15 AB53
GPIO_16 1 TPU25
GPIO_17 AA49
GPIO_18 AC48
GPIO_19 AE51 MEM_ID0 << PMU_INTR [48]
GPIO_20 AE49 MEM_ID1
GPIO_21 AC51 MEM_ID2
GPIO_22 AC49
GPIO_23 AA51 >> CNV_MFUART2_RXD [31]
GPIO_24 AA46
GPIO_25 AE41
GPIO_26 AE39
GPIO_27 AE46 << EMMC_BOOT STRAP [15]
GPIO_28 AE44 << SPI_BOOT STRAP [15]
GPIO_29 AC41 RU1 << BT_RF_KILL_N [11,31]
GPIO_30 AC39 HW_ID0
GPIO_31 AC44
GPIO_32 AC43 INT1_GSENSOR << INT1_GSENSOR [29]
GPIO_33 AA44 << SEN2_INT [29]
GPIO_34
GPIO_35 AA54
GPIO_36 AA53
GPIO_37 Y53 RU49 << SOC_WAKE_SCL_N [33]
GPIO_38 W54 << PMU_WAKE_N [33]
GPIO_39 W53
GPIO_40 Y53
GPIO_41
GPIO_105 L46
GPIO_134 H45
GPIO_135 H47 TOUCH_PAD_INT << TCH_PANEL_INT_N [26,29]
GPIO_136 L43 << TOUCH_PAD_INT [36]
GPIO_137 MA3 << CNV8_EN_N [31]
GPIO_138 H37 << CNV8_DISABLE_N [31]
GPIO_139 H43 << HW_ID2 [28]
GPIO_140 J43 << SATA0_DEVSLP [28]
GPIO_141 D43 << TCH_EN [26]
GPIO_142 F43 HW_ID1
GPIO_143 H41
GPIO_144 F39 << TCH_PANEL_RESET_N [26,29,33]
GPIO_145 L41 << SSD_RST_N [29]
GPIO_146 H27 RU3 << SLP_WLAN_N [31]
GPIO_210 U43 HW_ID5 << DMIC_SWITCH_CNT [37]
GPIO_212 U41 HW_ID6
GPIO_213 U39
GPIO_214



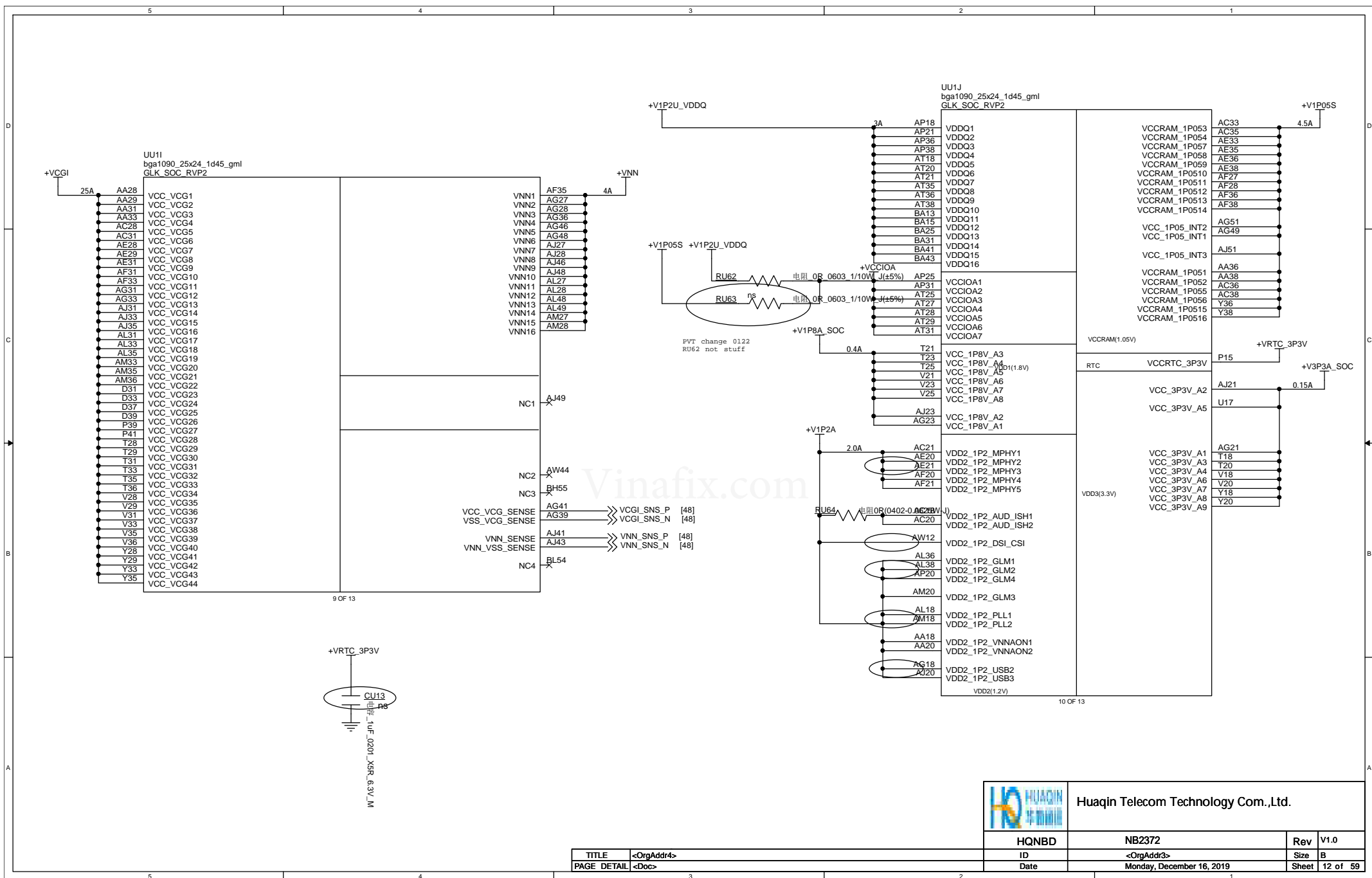
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bga1090_25x24_1d45_gml
GLK SOC RVP2

A3	VSS6	VSS53	AF44
A6	VSS13	VSS54	AF45
A12	VSS1	VSS55	AF47
A16	VSS2	VSS56	AF48
A20	VSS3	VSS57	AF50
A24	VSS4	VSS58	AF52
A28	VSS5	VSS59	AF53
A32	VSS6	VSS60	AF55
A36	VSS7	VSS64	AG20
A40	VSS8	VSS65	AL21
A44	VSS9	VSS66	AG25
A48	VSS10	VSS67	AG29
A51	VSS11	VSS68	AG35
AA12	VSS12	VSS69	AG38
AA13	VSS14	VSS70	AJ18
AA15	VSS15	VSS71	AJ25
AA17	VSS16	VSS72	AJ29
AA21	VSS17	VSS73	AJ36
AA23	VSS18	VSS74	AJ38
AA25	VSS19	VSS75	AJ39
AA27	VSS20	VSS76	AJ44
AA35	VSS21	VSS77	AK1
AA43	VSS22	VSS78	AK3
AA48	VSS23	VSS79	AK55
AB1	VSS24	VSS80	AL3
AB3	VSS25	VSS81	AL7
AB55	VSS26	VSS82	AL8
AC8	VSS27	VSS83	AL10
AC13	VSS28	VSS84	AL12
AC23	VSS29	VSS85	AL13
AC25	VSS30	VSS86	AL17
AC27	VSS31	VSS87	AL20
AC29	VSS32	VSS88	AL25
AE18	VSS33	VSS89	AL29
AE23	VSS34	VSS90	AL39
AE25	VSS35	VSS91	AL41
AE27	VSS36	VSS92	AL43
AE43	VSS37	VSS93	AL44
AE48	VSS38	VSS94	AL46
AF1	VSS39	VSS95	AL51
AF3	VSS40	VSS96	AM1
AF4	VSS41	VSS97	AM21
AF6	VSS42	VSS98	AM23
AF8	VSS43	VSS99	AM25
AF9	VSS44	VSS100	AM29
AF11	VSS45	VSS101	AM31
AF12	VSS46	VSS102	AM38
AF14	VSS47	VSS103	AM55
AF16	VSS48	VSS104	AN3
AF18	VSS49	VSS105	AN8
AF23	VSS50	VSS106	AN10
AF25	VSS51	VSS107	AN46
AF29	VSS52	VSS109	
AF40			
AF42			
VSS52			

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GLK SOC RVP2

AN48	VSS_111	VSS_165	BC11
AN49	VSS_112	VSS_166	BC17
AN51	VSS_113	VSS_167	BC19
AN53	VSS_114	VSS_168	BC21
AP23	VSS_115	VSS_169	BC23
AP27	VSS_116	VSS_170	BC25
AP28	VSS_117	VSS_171	BC31
AP29	VSS_118	VSS_172	BC33
AP35	VSS_119	VSS_173	BC35
AR2	VSS_120	VSS_174	BC37
AR7	VSS_121	VSS_175	BC39
AR10	VSS_122	VSS_176	BC41
AR12	VSS_123	VSS_177	BC45
AR44	VSS_124	VSS_178	BC51
AR49	VSS_125	VSS_179	BD9
AR54	VSS_126	VSS_180	BD15
AT23	VSS_127	VSS_181	BD19
AT33	VSS_128	VSS_182	BD21
AT39	VSS_129	VSS_183	BD28
AU3	VSS_130	VSS_184	BD35
AU10	VSS_131	VSS_185	BD37
AU28	VSS_132	VSS_186	BD47
AU33	VSS_133	VSS_187	BE3
AU46	VSS_134	VSS_188	BE28
AV15	VSS_135	VSS_189	BE53
AV17	VSS_136	VSS_190	BF9
AV23	VSS_137	VSS_191	BF19
AV25	VSS_138	VSS_192	BF37
AV31	VSS_139	VSS_193	BF47
AV33	VSS_140	VSS_194	BG1
AV39	VSS_141	VSS_195	BG6
AW2	VSS_142	VSS_196	BG28
AW5	VSS_143	VSS_197	BG50
AW10	VSS_144	VSS_198	CG55
AW28	VSS_145	VSS_199	F1
AW46	VSS_146	VSS_200	F4
AW51	VSS_147	VSS_201	BH11
AW64	VSS_148	VSS_202	BH13
AY13	VSS_149	VSS_203	BH17
AY15	VSS_150	VSS_204	BH19
AY28	VSS_151	VSS_205	BH23
AY41	VSS_152	VSS_206	BH25
AY43	VSS_153	VSS_207	BH28
B2	VSS_154	VSS_208	BH31
B55	VSS_155	VSS_209	BH33
BA27	VSS_156	VSS_210	BH37
BA29	VSS_157	VSS_211	BH39
BB1	VSS_158	VSS_212	BH41
BB28	VSS_159	VSS_213	BH45
BB55	VSS_160	VSS_214	BJ2
BC5	VSS_161	VSS_215	BJ15
	VSS_162	VSS_216	BJ19
	VSS_163	VSS_217	BJ25
	VSS_164	VSS_218	BJ28
	VSS_165	VSS_219	BJ31
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GLK SOC RVP2

AL23	VSS1	VSS51	J51
BJ54	VSS2	VSS52	K1
BK1	VSS3	VSS53	K3
BK17	VSS4	VSS54	K28
BK21	VSS5	VSS55	K55
BK35	VSS6	VSS56	L5
BK39	VSS7	VSS57	L7
BK55	VSS8	VSS58	L8
BL5	VSS9	VSS59	L19
BL8	VSS10	VSS60	L33
BL10	VSS11	VSS61	L39
BL14	VSS12	VSS62	M15
BL24	VSS13	VSS63	M25
BL28	VSS14	VSS64	M28
BL32	VSS15	VSS65	M35
BL42	VSS16	VSS66	M41
BL46	VSS17	VSS67	N12
BL48	VSS18	VSS68	N28
BL51	VSS19	VSS69	N46
C1	VSS20	VSS70	N51
C12	VSS21	VSS71	P21
C16	VSS22	VSS72	P55
C28	VSS23	VSS73	R8
C36	VSS24	VSS74	R28
D6	VSS25	VSS75	T27
D9	VSS26	VSS76	T38
D21	VSS27	VSS77	U13
D28	VSS28	VSS78	V27
D41	VSS29	VSS79	V38
D45	VSS30	VSS80	V45
D55	VSS31	VSS81	W2
E28	VSS32	VSS82	W3
E50	VSS33	VSS83	W5
E55	VSS34	VSS84	W7
F1	VSS35	VSS85	W8
F4	VSS36	VSS86	W10
F21	VSS37	VSS87	W39
F31	VSS38	VSS88	W41
G28	VSS39	VSS89	W43
H13	VSS40	VSS90	W44
H15	VSS41	VSS91	W46
H21	VSS42	VSS92	W48
H23	VSS43	VSS93	W49
H28	VSS44	VSS94	W51
H33	VSS45	VSS95	Y21
H39	VSS46	VSS96	Y23
J8	VSS47	VSS97	Y25
J27	VSS48	VSS98	Y27
J33	VSS49	VSS99	Y31
J41	VSS50	VSS100	Y33
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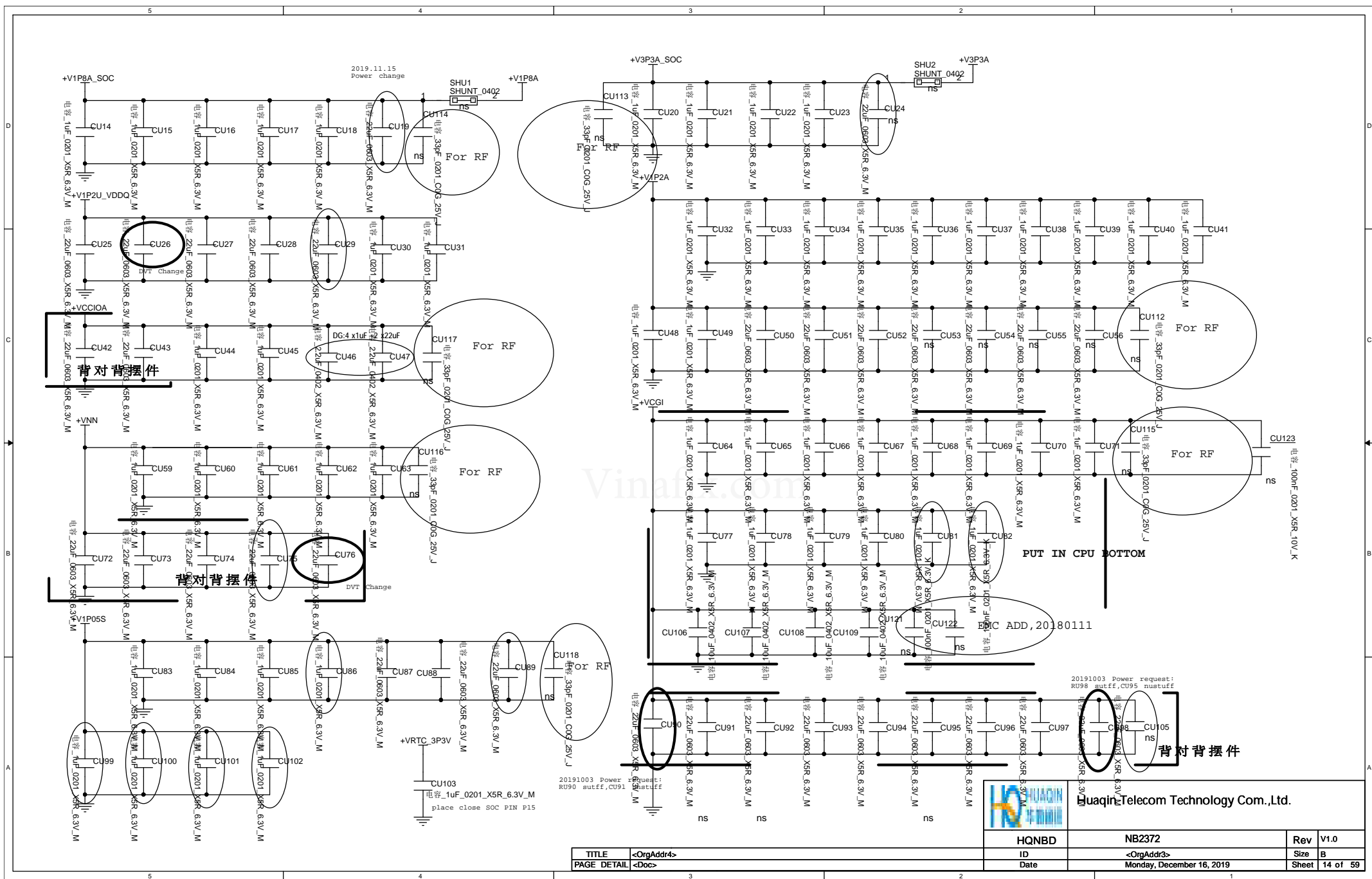
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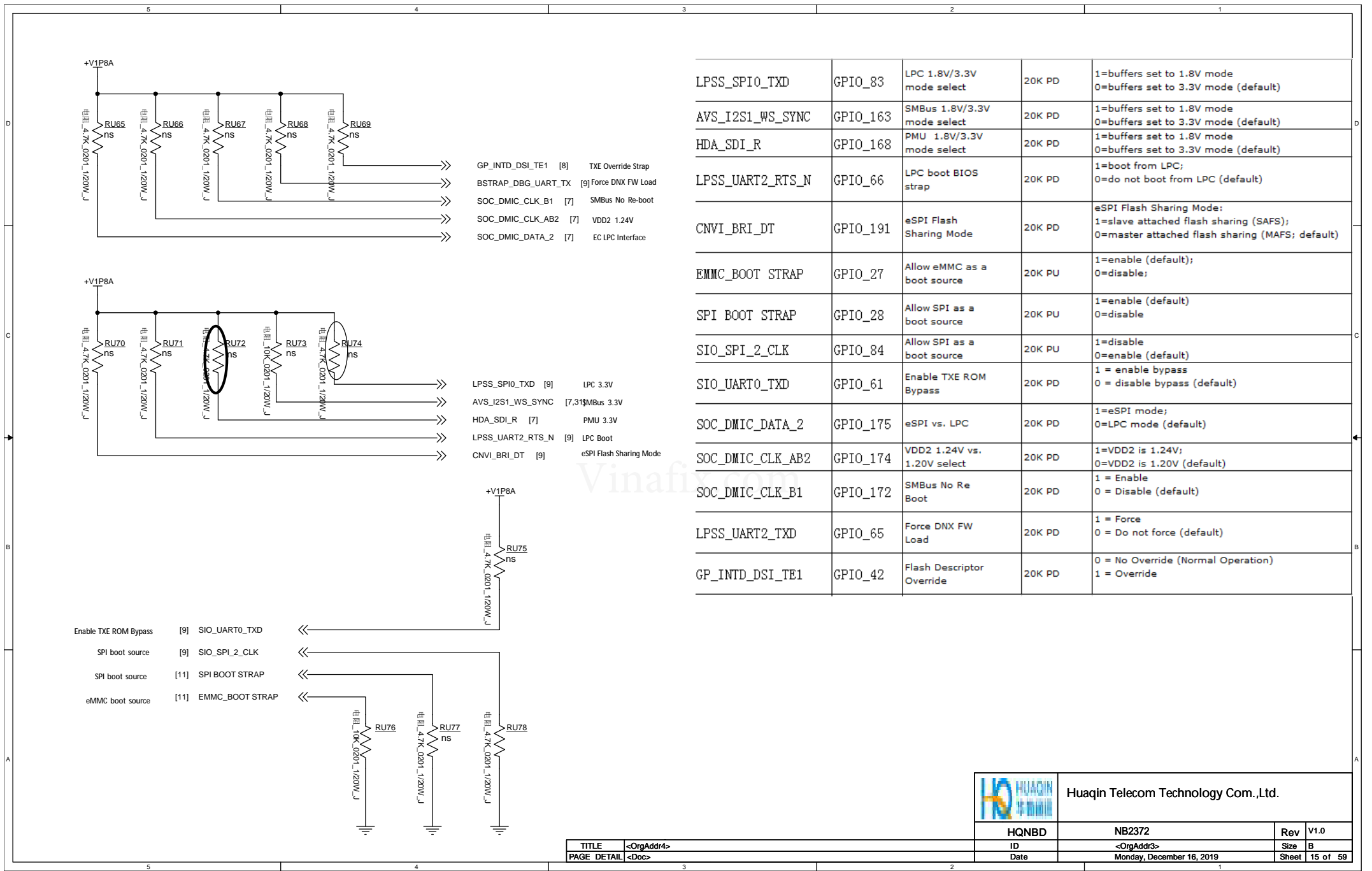
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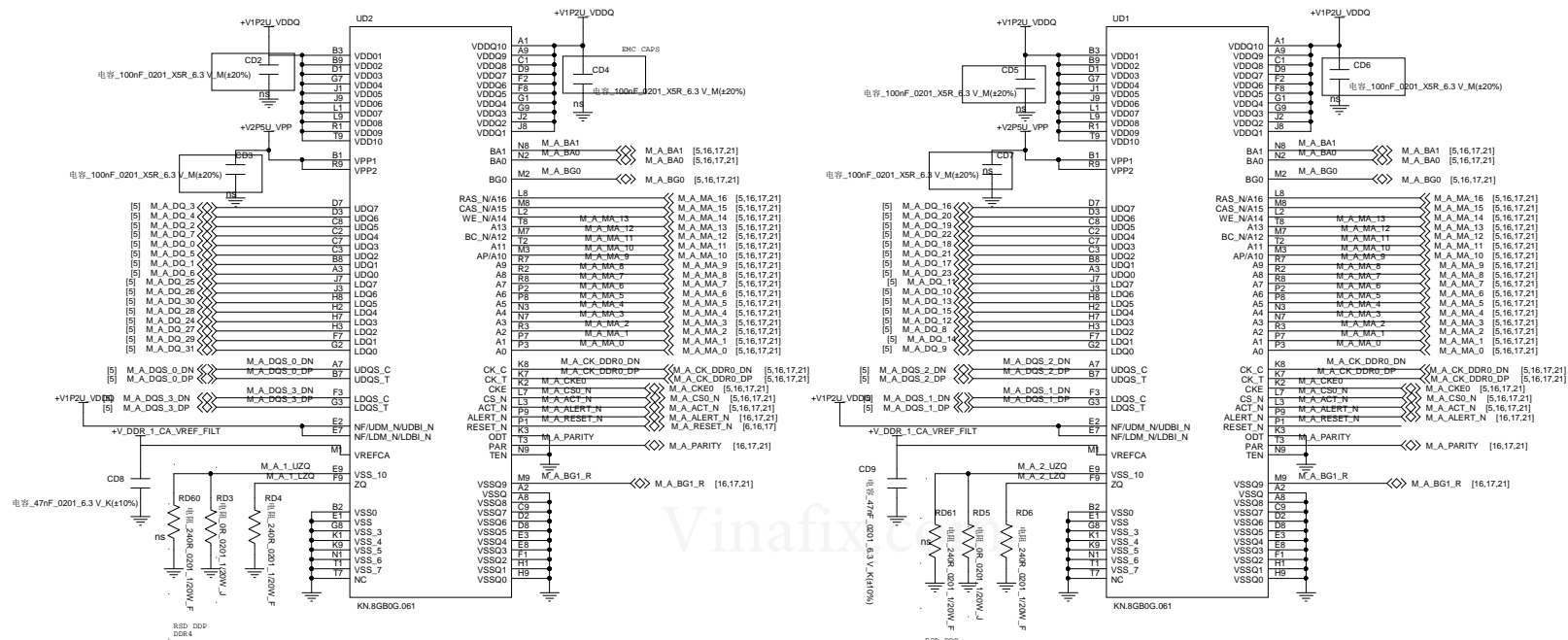


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NOTE: TO BE STUFF FOR DUAL ZQ PARTS



BOM NOTE

DDR PINS	SDP	DDP
E9	UZQ	GND
M9	BG1	GND



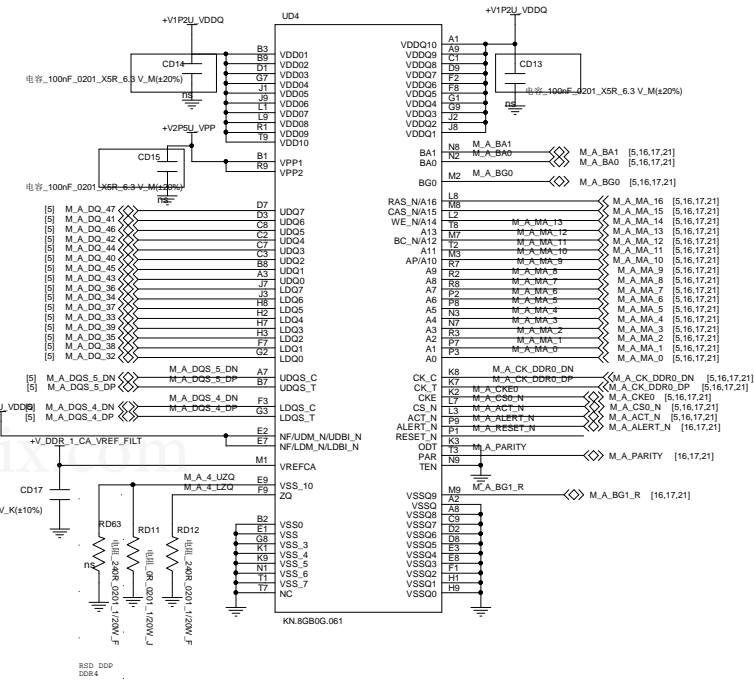
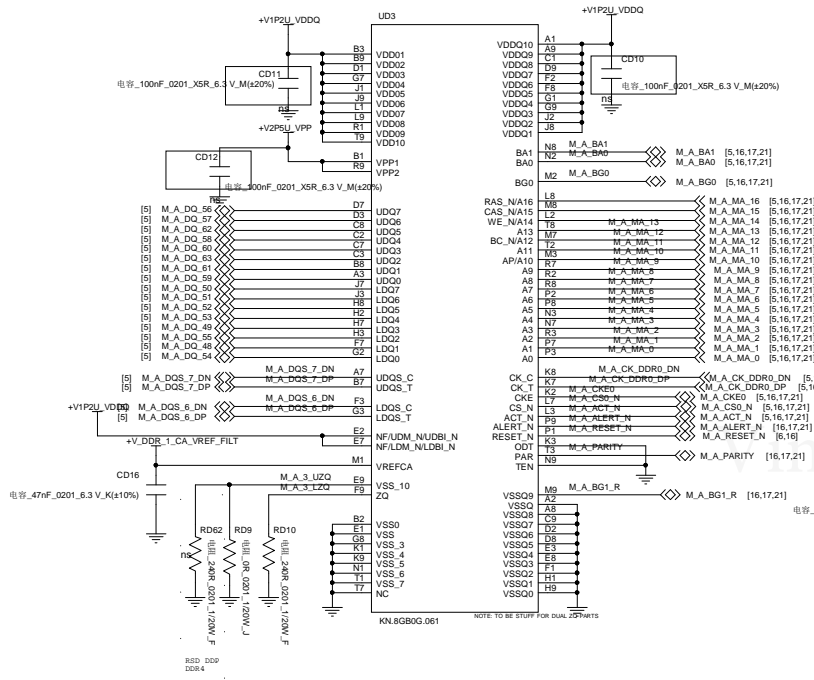
Huaqin Telecom Technology Co., Ltd.

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ID

NB2372
Date

Rev V1.0
<Original>
Monday, December 16, 2019
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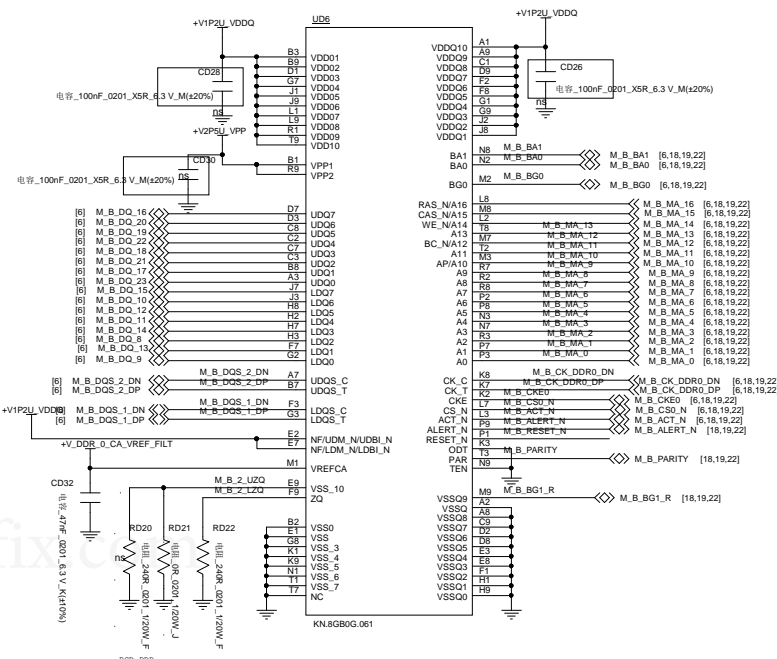
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TITLE: -Original-
PAGE: DETAIL -Dwg-

HQNB
ID

NB2372
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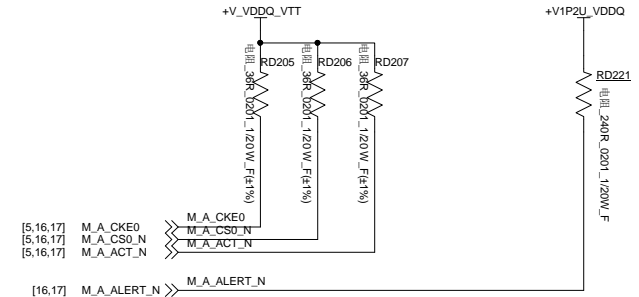
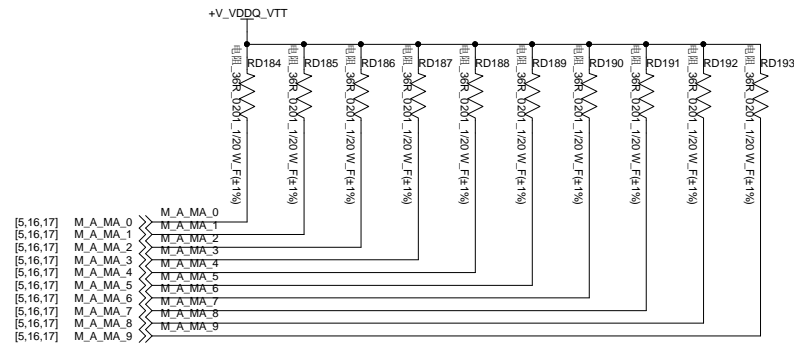
BOM NOTE

DDR PINS		SDP	DDP
E9	UZQ	GND	240E PD

DDR PINS		SDP	DDP
E9	UZQ	GND	240E PD
M9	BG1	GND	BG1 SIG FROM CONTROLLER

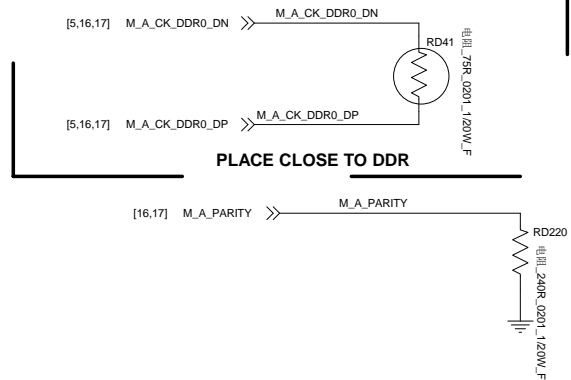
The schematic shows the power supply circuitry. It includes two main input rails: +V1P2U_VDDQ and +V1P2U_VDDQ. The +V1P2U_VDDQ rail is connected to a network of resistors (RD213, RD214, RD181) and capacitors (CD254, CD280). A specific voltage divider is shown with RD213 (3.65K_0201_1/20W_F) and RD214 (3.65K_0201_1/20W_F) connected to +V1P2U_VDDQ, and RD181 (24.9R_0201_1/20W_F(±1%)) connected to ground. The output of this divider is labeled +V_DDR_1_CA_VREF. Another capacitor CD280 (22nF_0201_XSR_6.3V_K) is connected between +V_DDR_1_CA_VREF and ground. The +V_DDR_1_CA_VREF signal is also connected to the VDD pin of the ADXL05 IC.

MEMORY TERMINATIONS MD CHANNEL A



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PLACE TERMINATION RESISTOR CLOSE TO LAST CHIP



PLACE CLOSE TO DDR

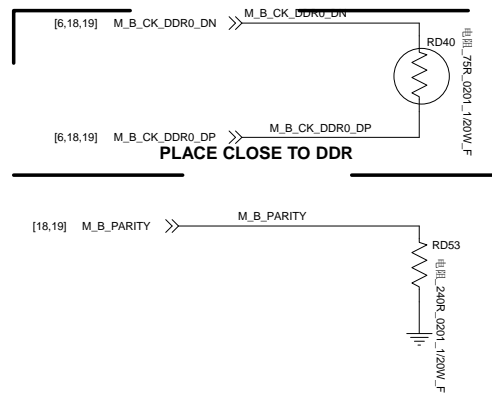
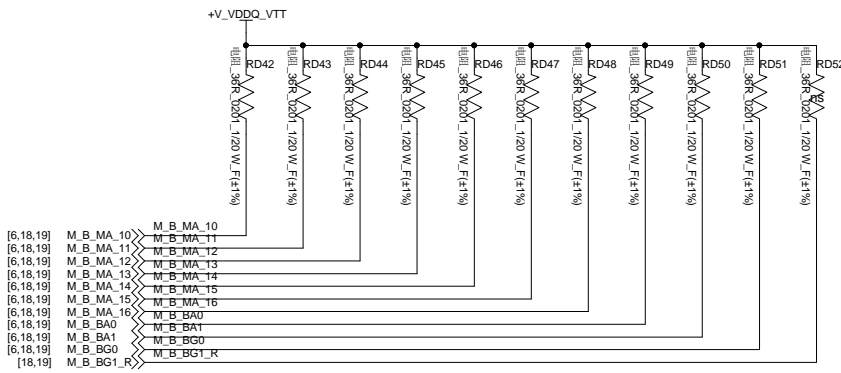
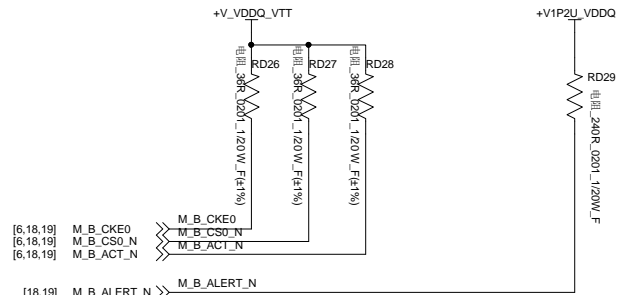
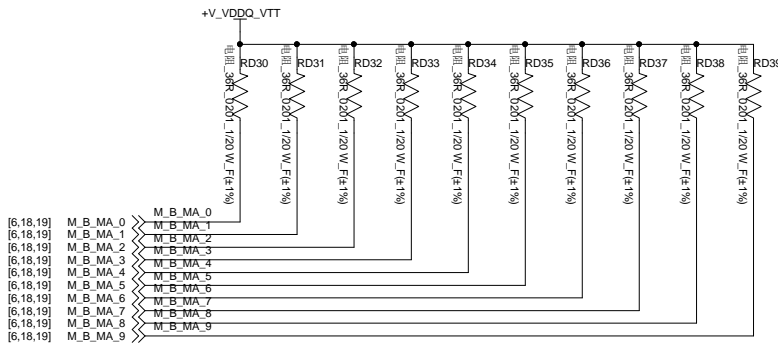


Huaqin Telecom Technology Co.,Ltd.

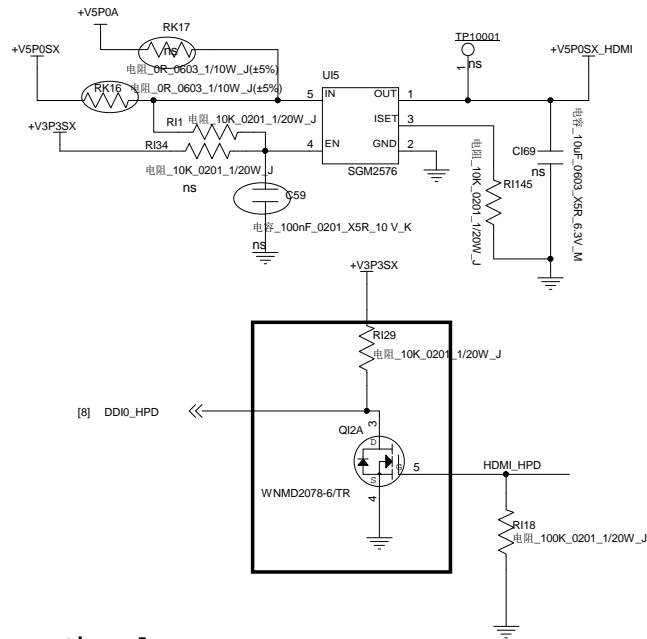
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Date	Monday, December 16, 2019	Sheet	21 of 59

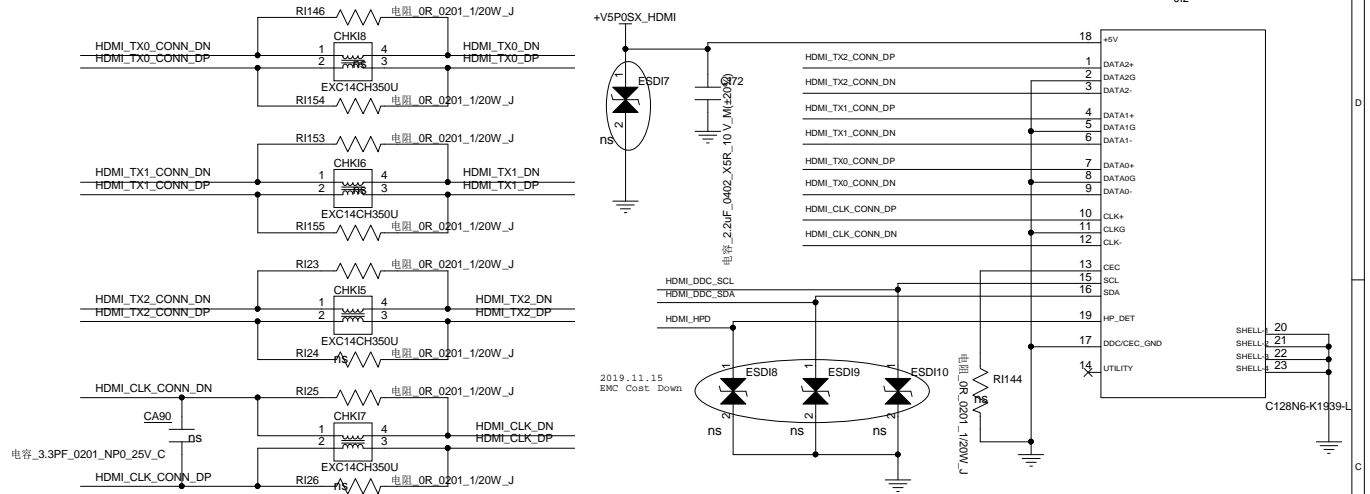
MEMORY TERMINATIONS MD CHANNEL B



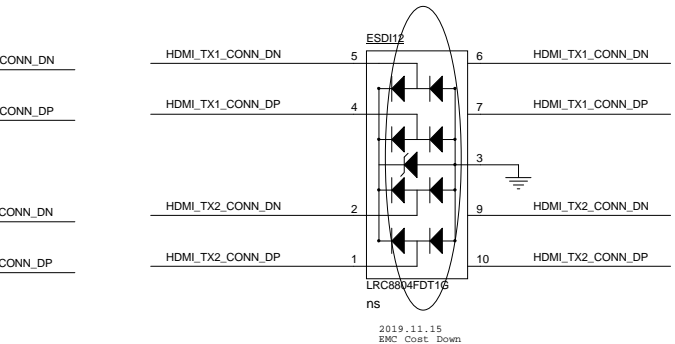
Power 1



HDMI CONN

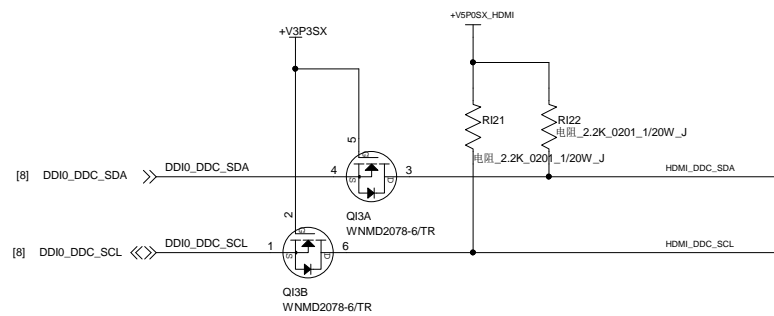
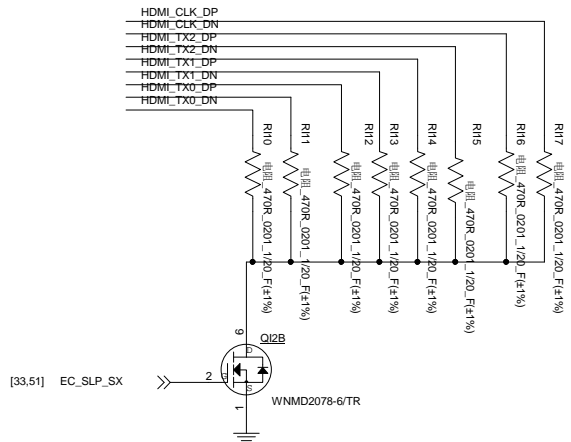



ESD



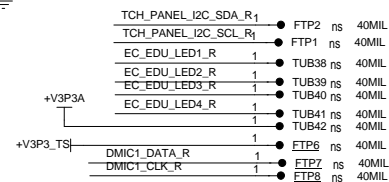
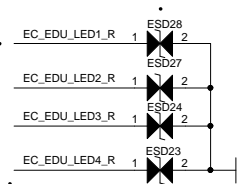
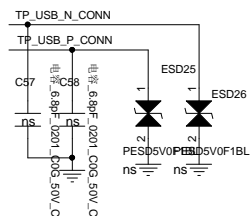
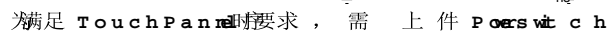
Signal

[8] DDIO_TX0_DN	电容 100nF_0201_X5R_10V_K	C161	HDMI_TX2_DN
[8] DDIO_TX0_DP	电容 100nF_0201_X5R_10V_K	C171	HDMI_TX2_DP
[8] DDIO_TX1_DN	电容 100nF_0201_X5R_10V_K	C163	HDMI_TX1_DN
[8] DDIO_TX1_DP	电容 100nF_0201_X5R_10V_K	C164	HDMI_TX1_DP
[8] DDIO_TX2_DN	电容 100nF_0201_X5R_10V_K	C165	HDMI_TX0_DN
[8] DDIO_TX2_DP	电容 100nF_0201_X5R_10V_K	C166	HDMI_TX0_DP
[8] DDIO_TX3_DN	电容 100nF_0201_X5R_10V_K	C167	HDMI_CLK_DN
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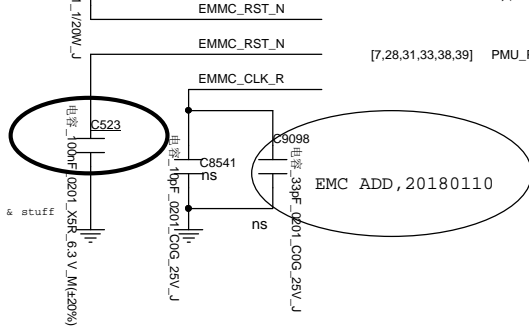
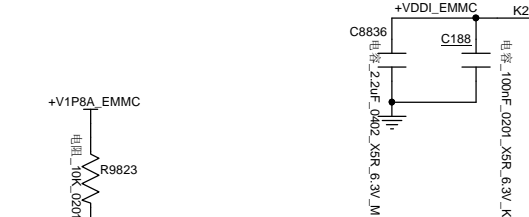
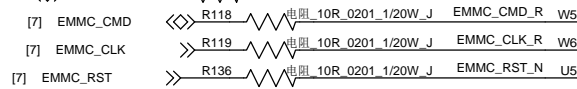
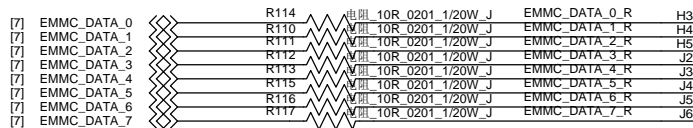
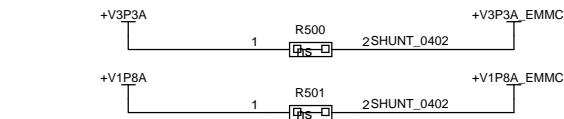
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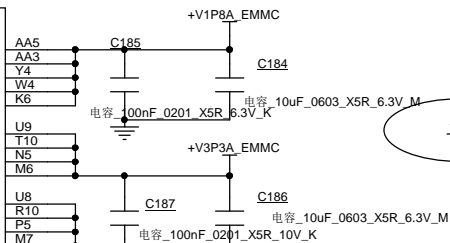
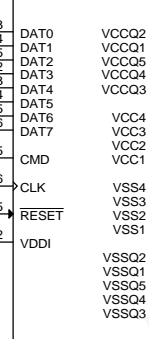
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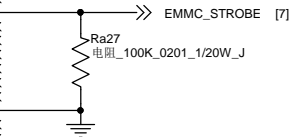
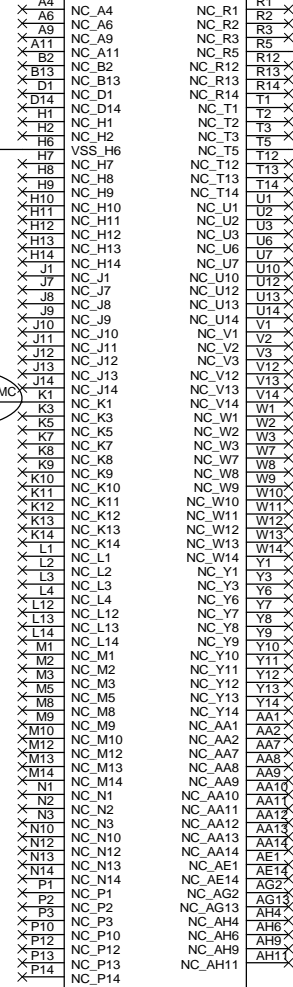
0116 PVT:
Change to 0.1uF & stuff

EMC ADD, 20180110

U7A
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U7B
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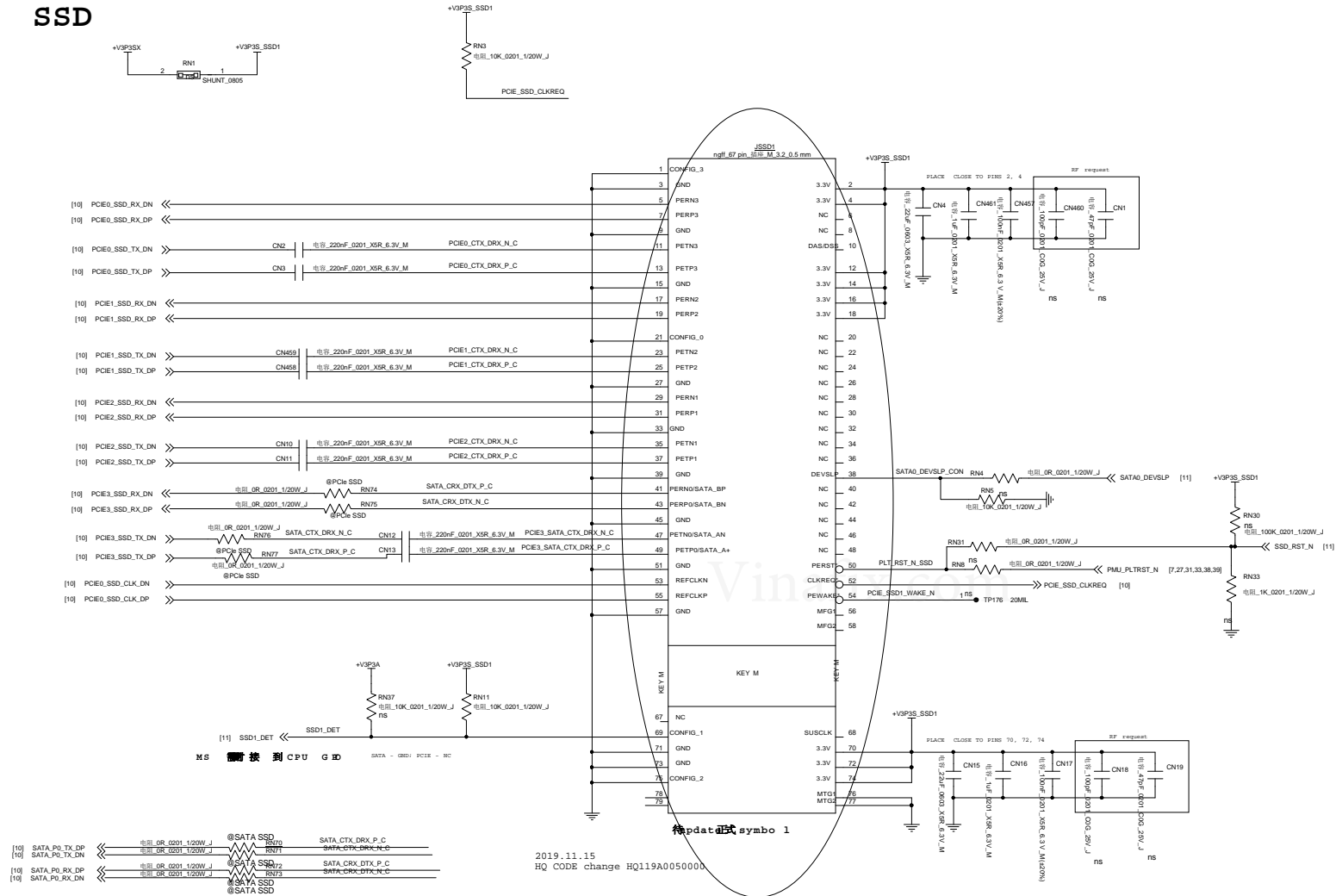


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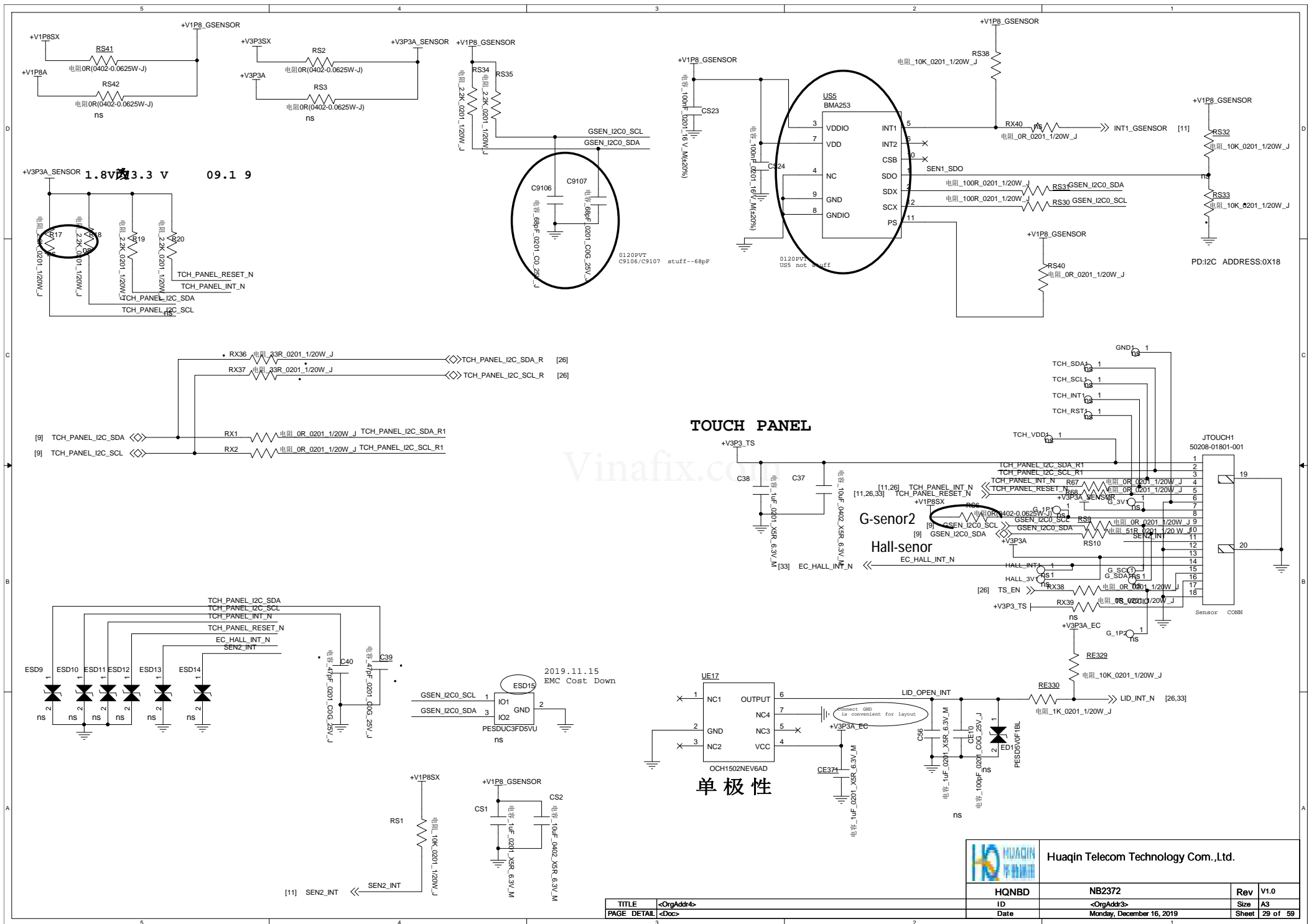
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HQNB	NB2372	Rev	V1.0
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SSD



[10] SATA_P0_TX_DP	电阻 0R_0201_1/20W_J	@SATA SSD	SATA_CTX_DRX_P_C
[10] SATA_P0_TX_DN	电阻 0R_0201_1/20W_J	RN70	SATA_CTX_DRX_N_C
[10] SATA_P0_RX_DP	电阻 0R_0201_1/20W_J	@SATA SSD	SATA_CTX_DRX_P_C
[10] SATA_P0_RX_DN	电阻 0R_0201_1/20W_J	RN71	SATA_CTX_DRX_N_C



5

4

3

2

1

D

D

C

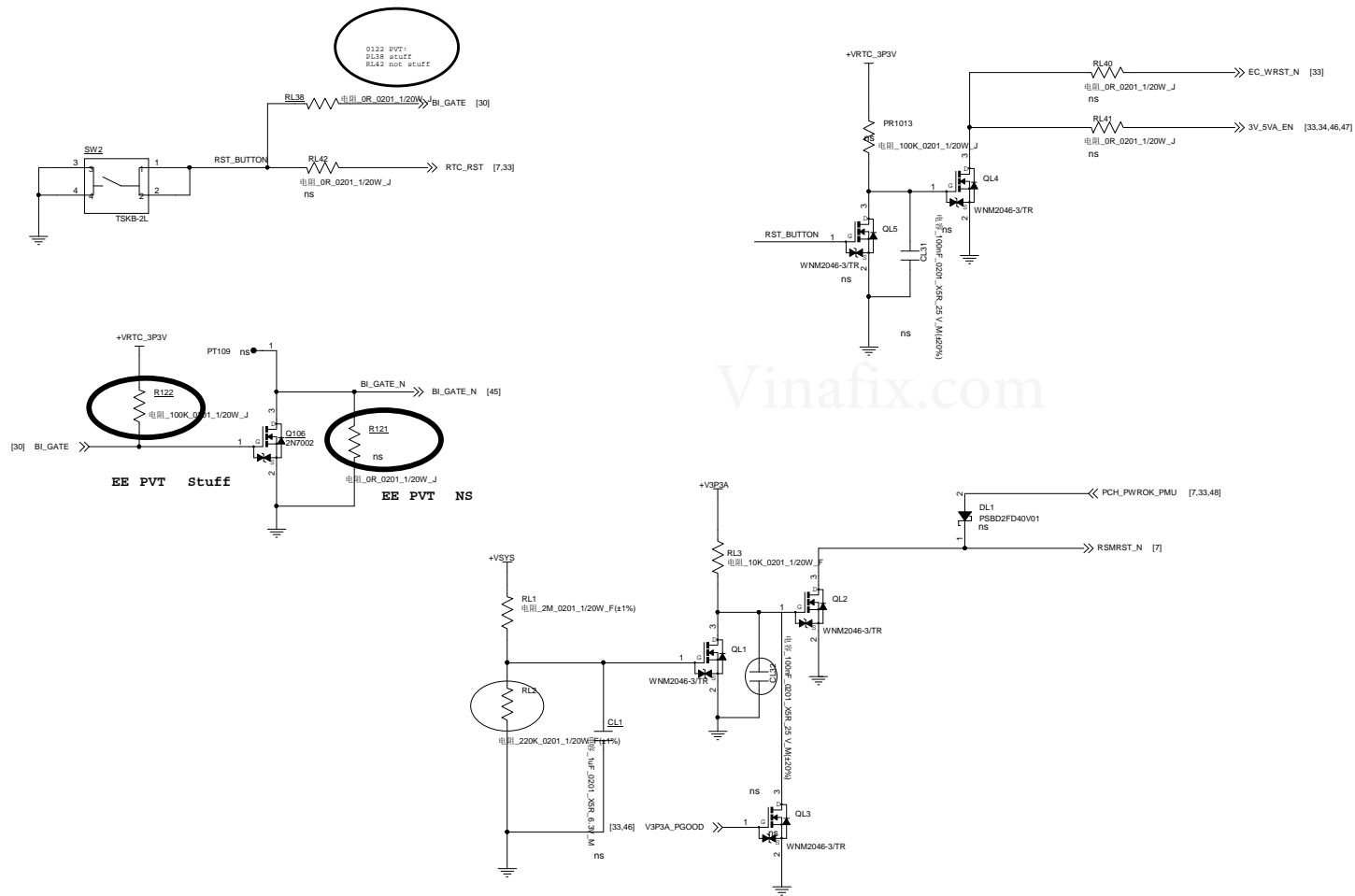
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B

B

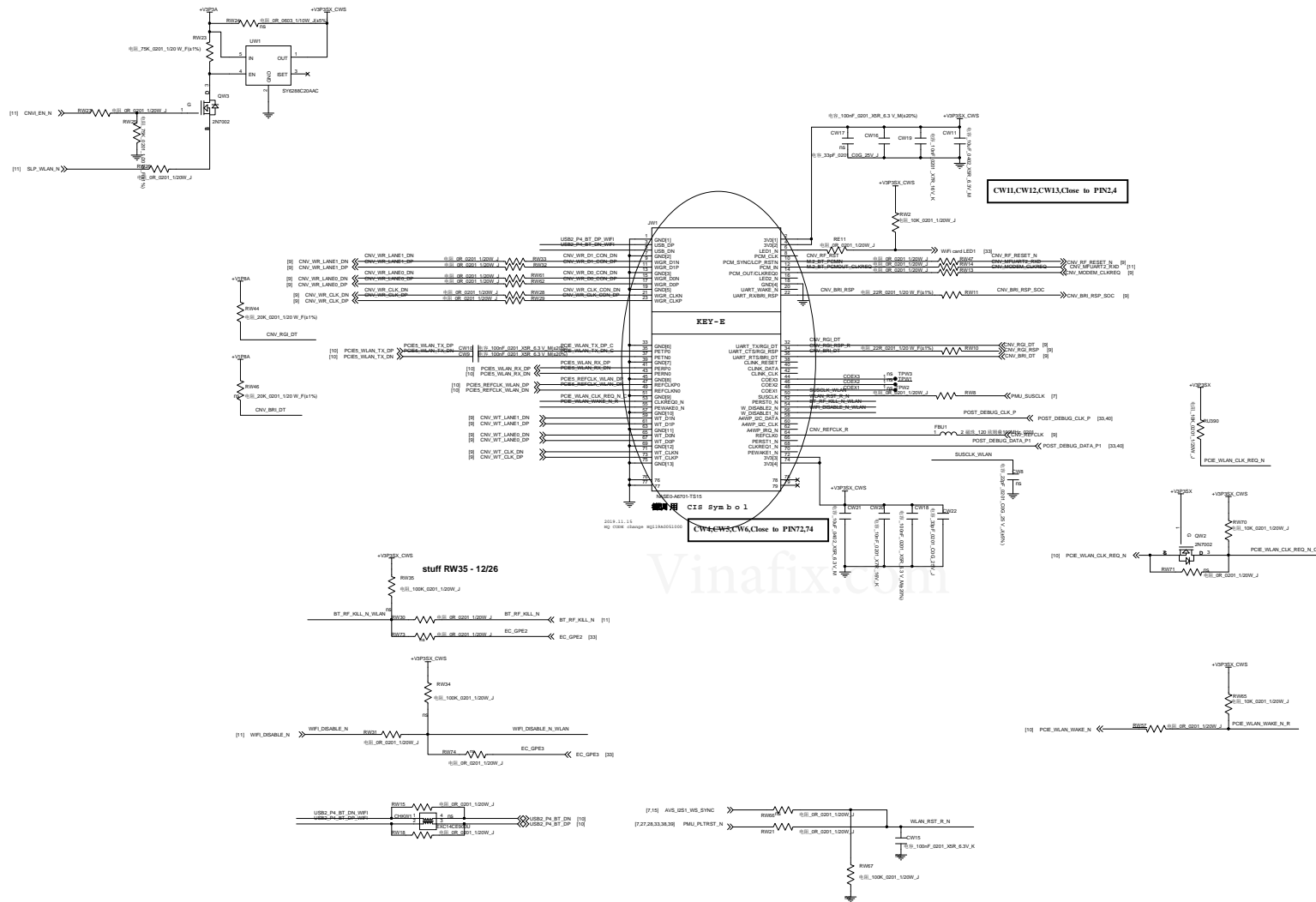
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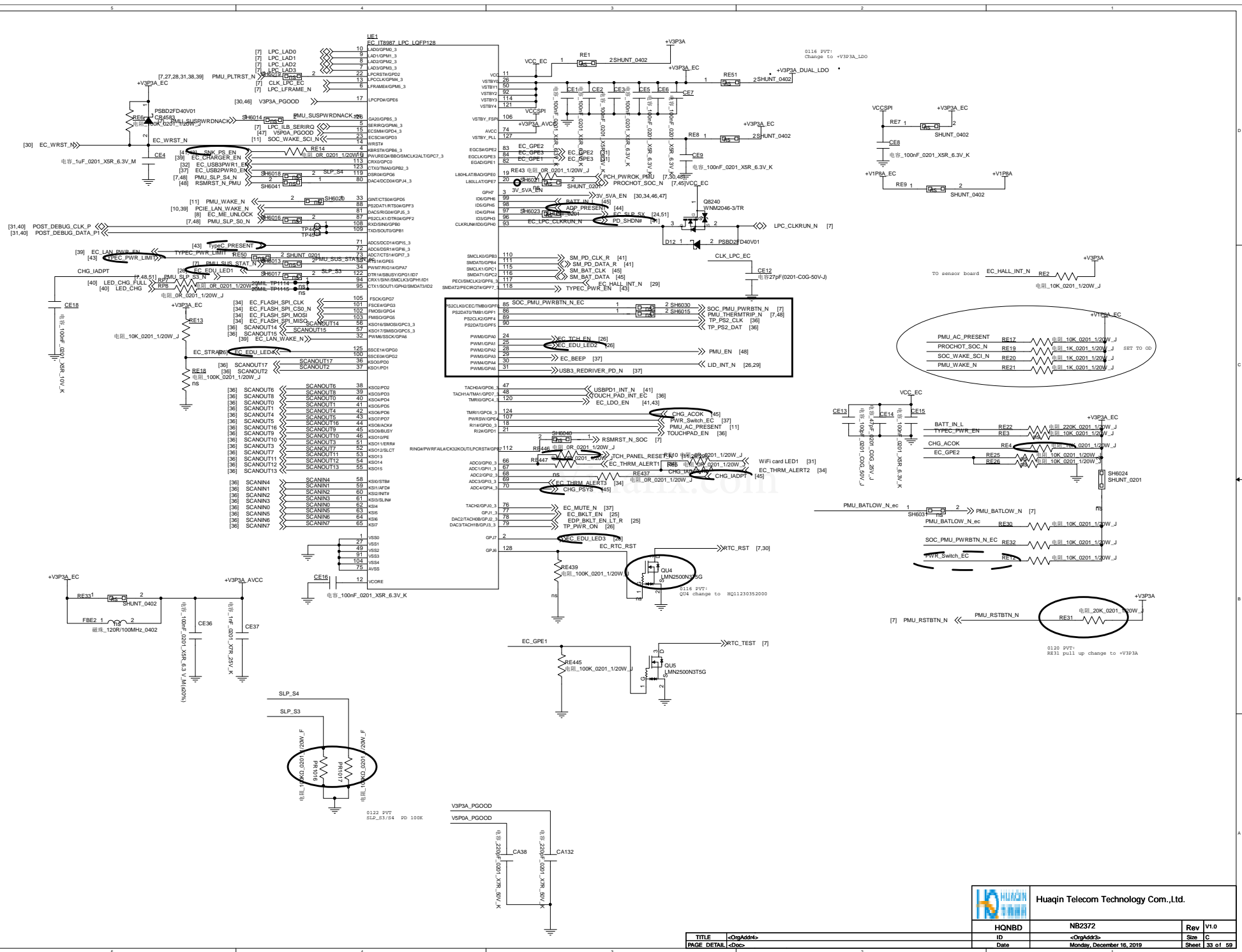
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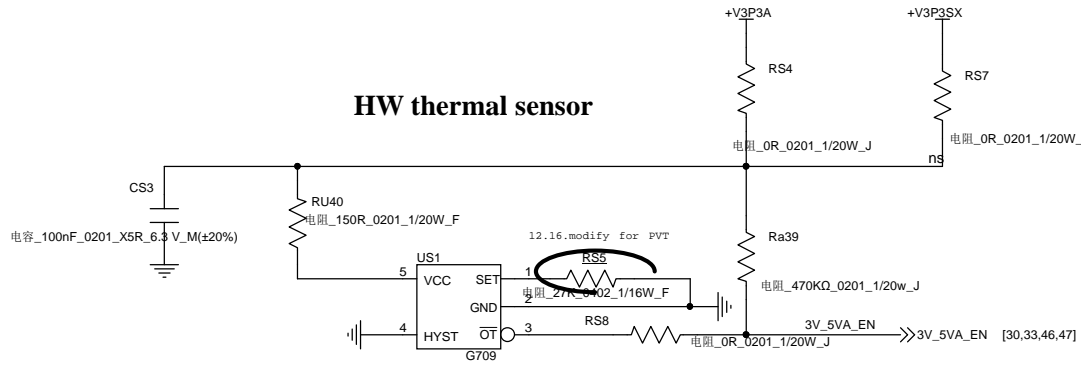
Huaqin Telecom Technology Co., Ltd.

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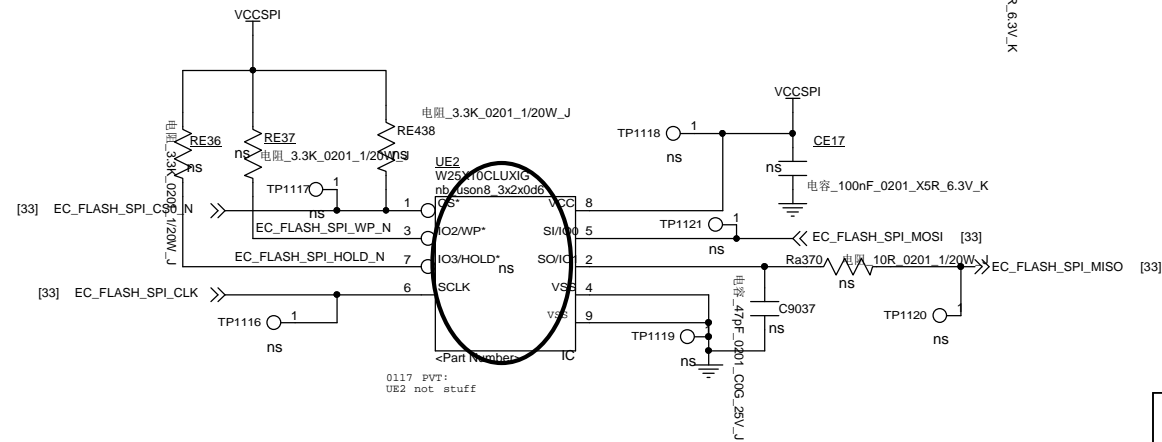
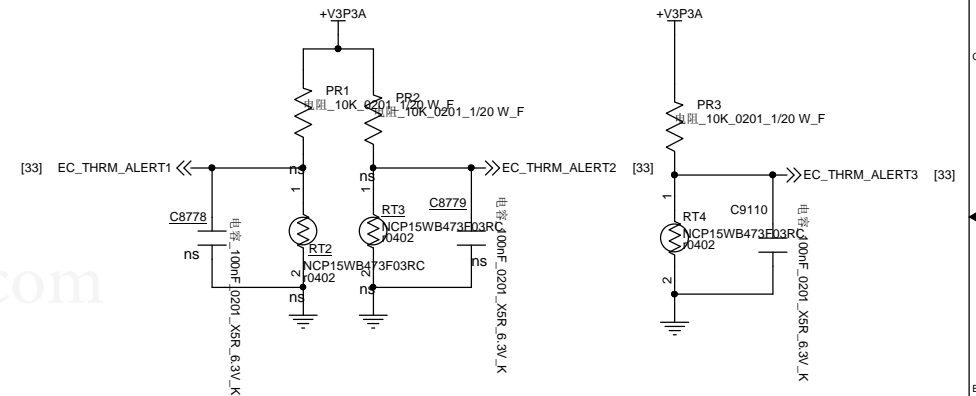



HW thermal sensor



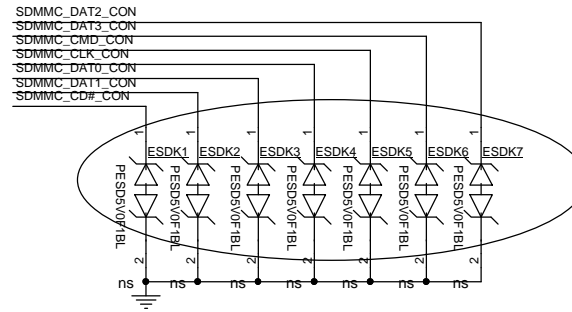
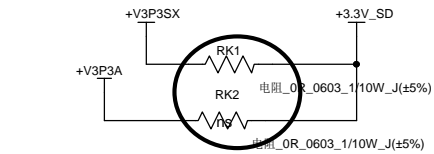
NOTE:
HW thermal sensor??

US1 For HW Shutdown close to +VCGI

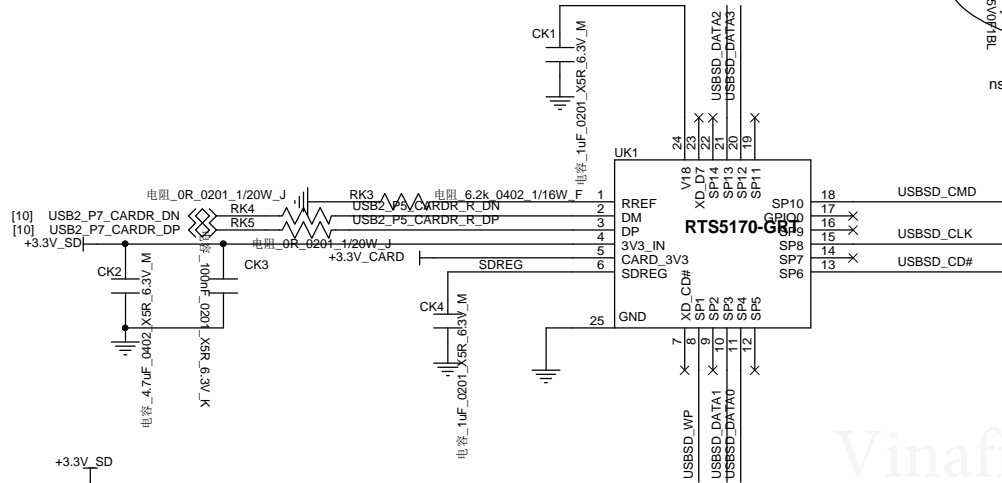
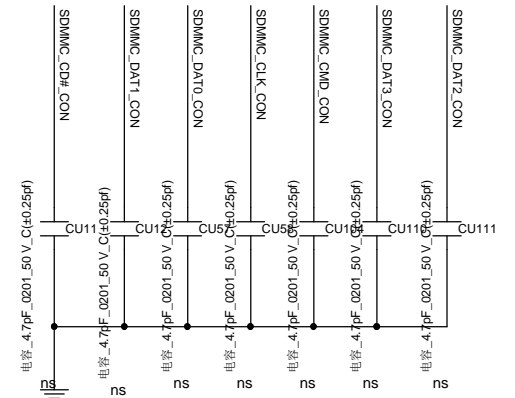


			
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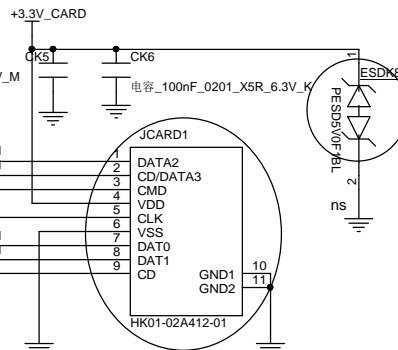
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2019.11.15
EMC Cost Down




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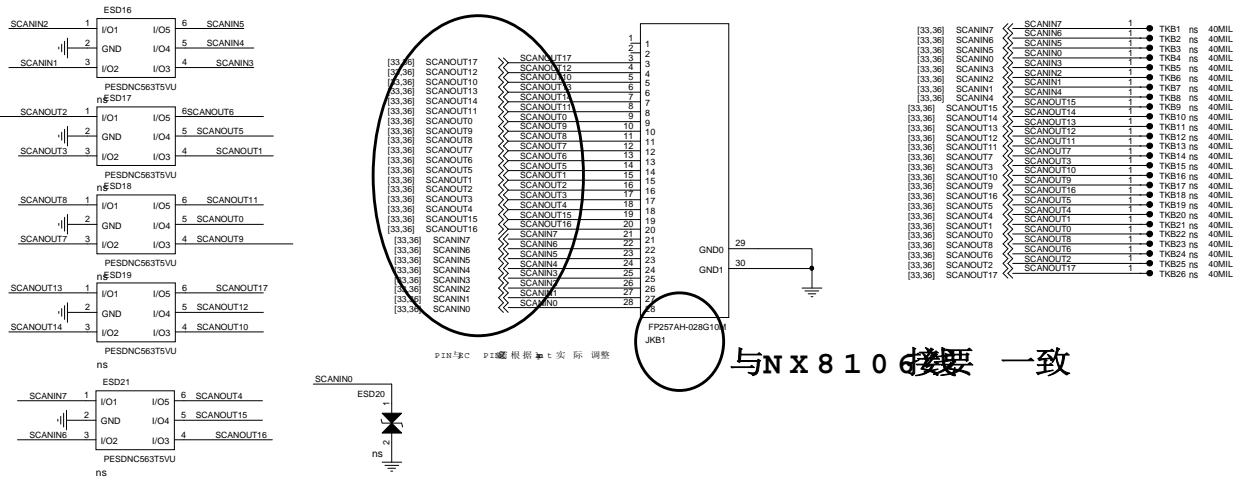
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HQ CODE change HQ11960603000

2019.11.15
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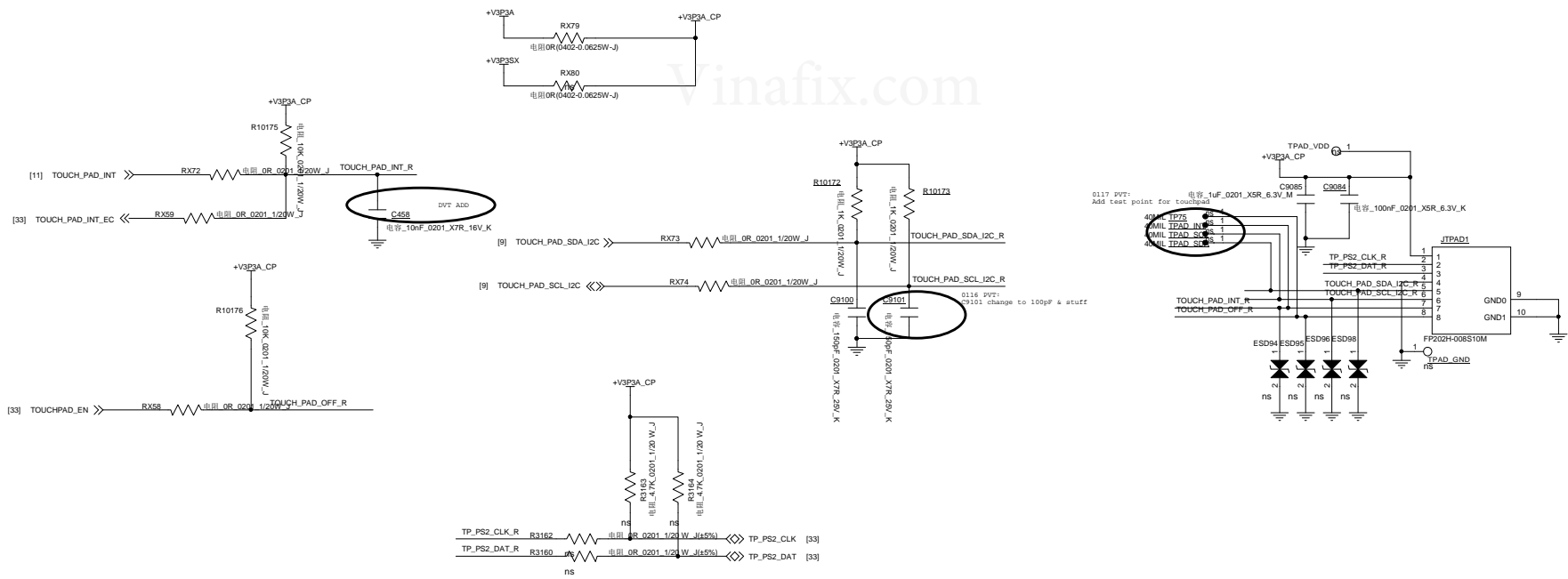
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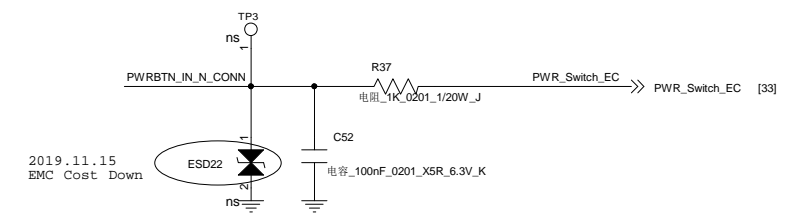
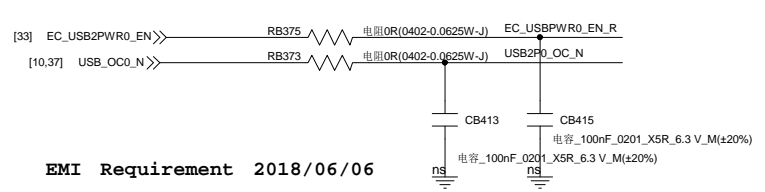
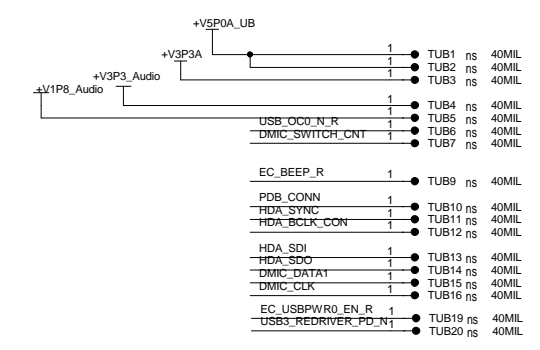
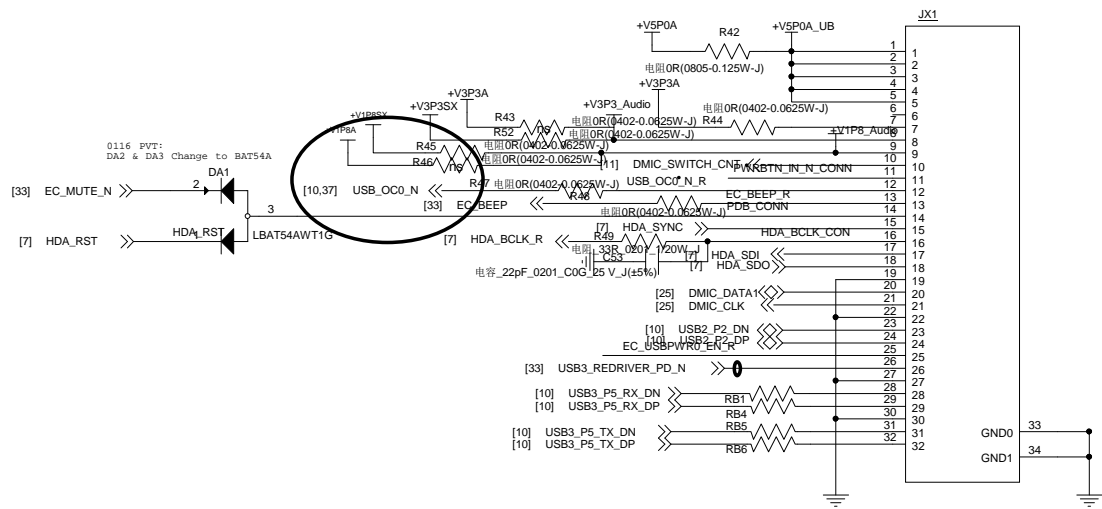
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KEY Board



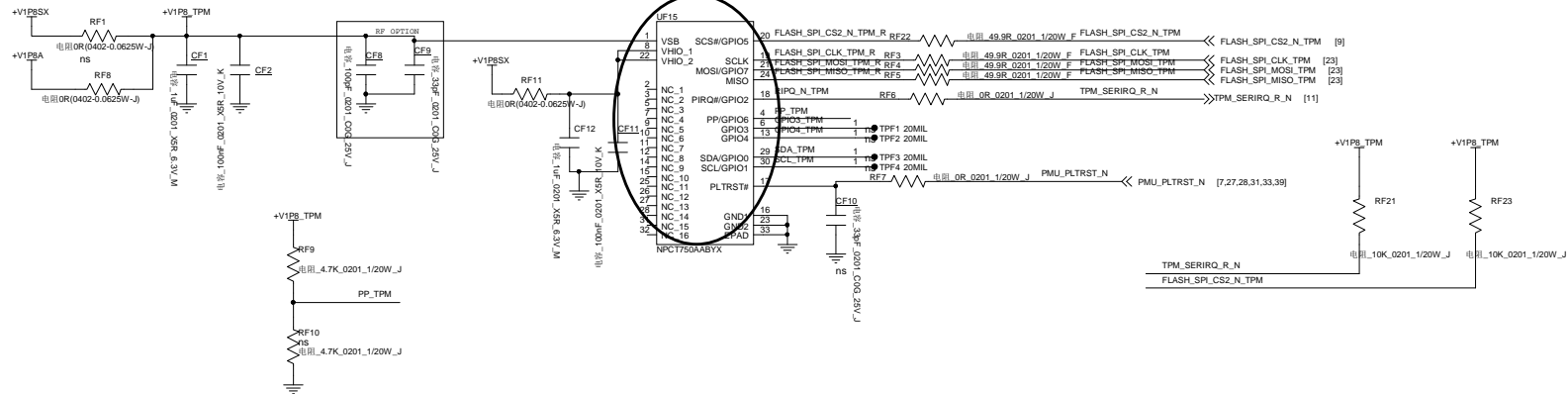
Touch Pad





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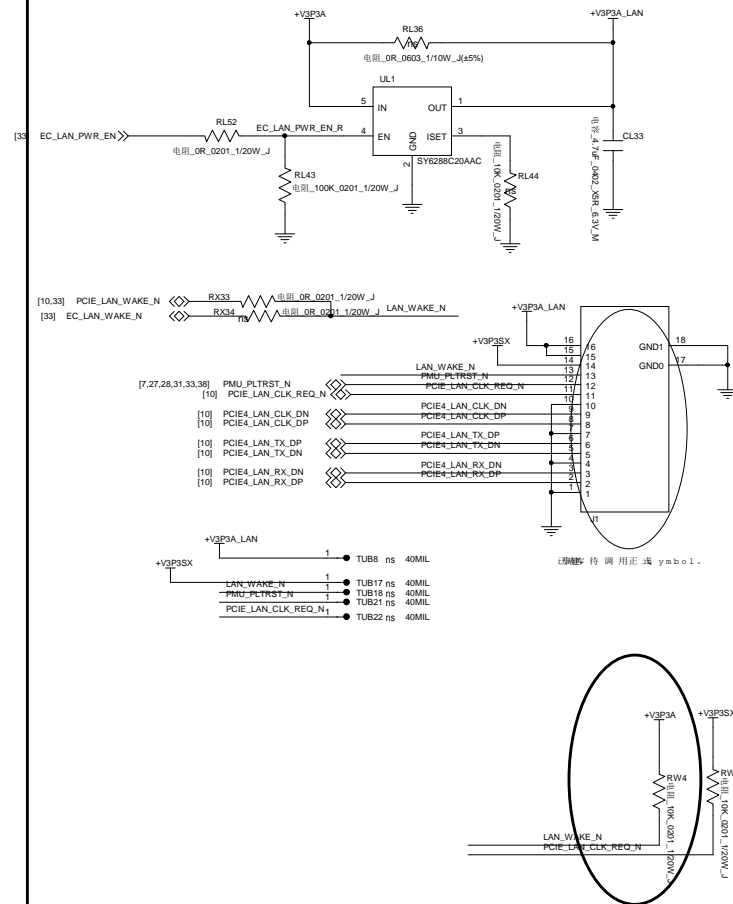
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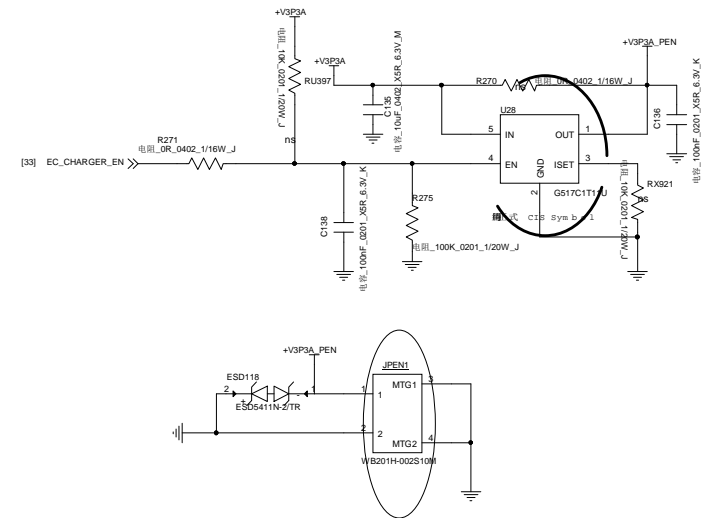
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RJ45 CONN

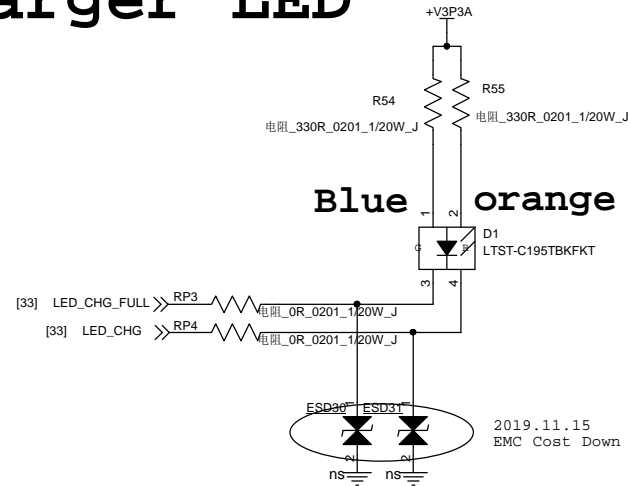
Suport S5 LAN WAKE



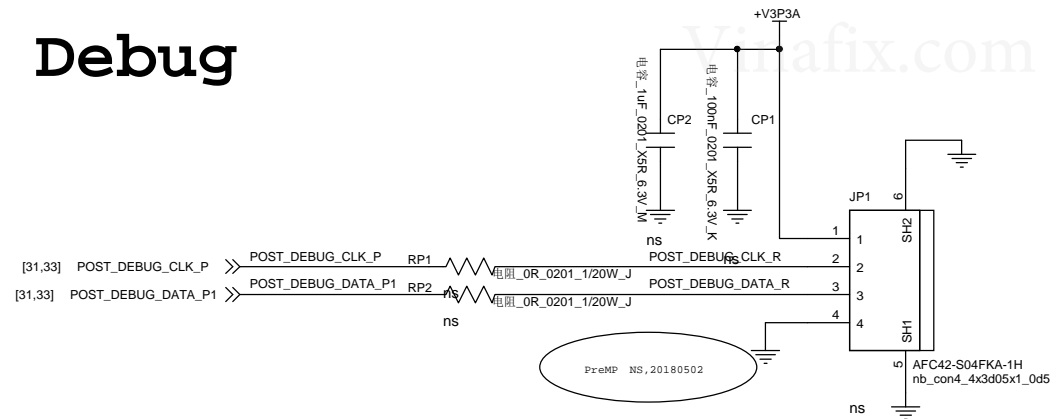
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Charger LED

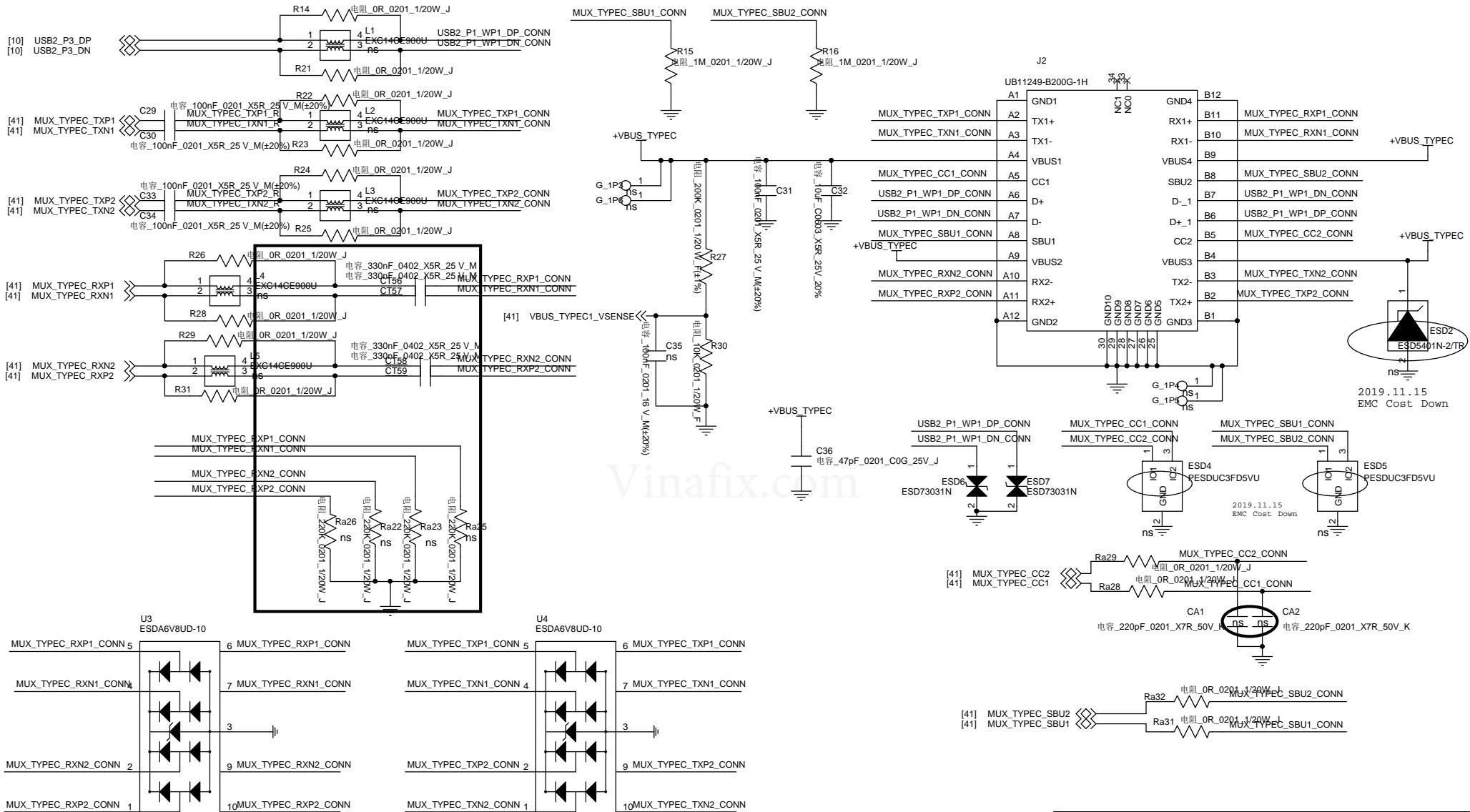


Debug




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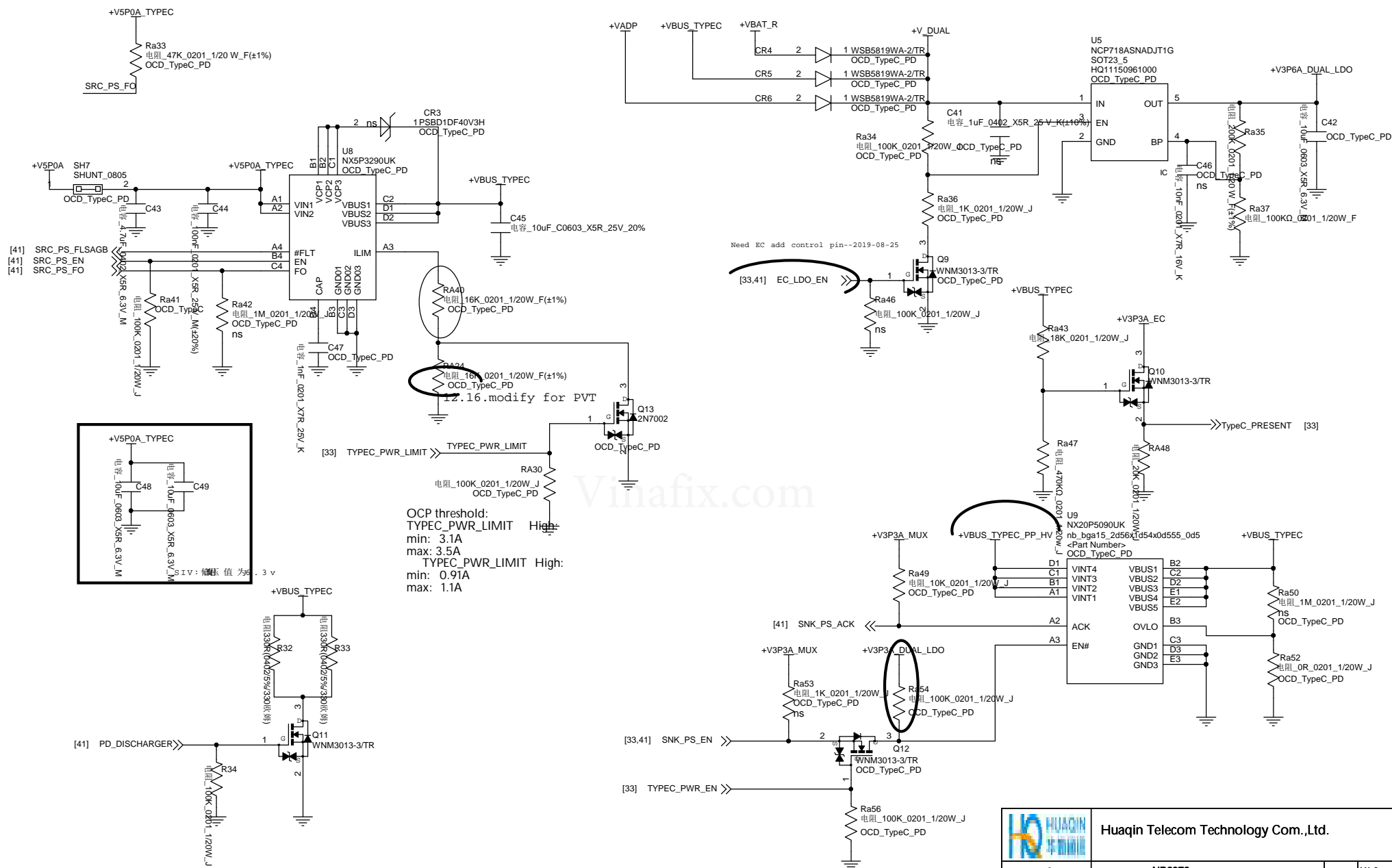
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PAGE DETAIL	<Doc>



Placing MLCC's symmetrically
on the top- and bottom-sides

Placing MLCC's symmetrically
on the top- and bottom-sides

```

Voltage : 20V
Ilimit  : 3.1A

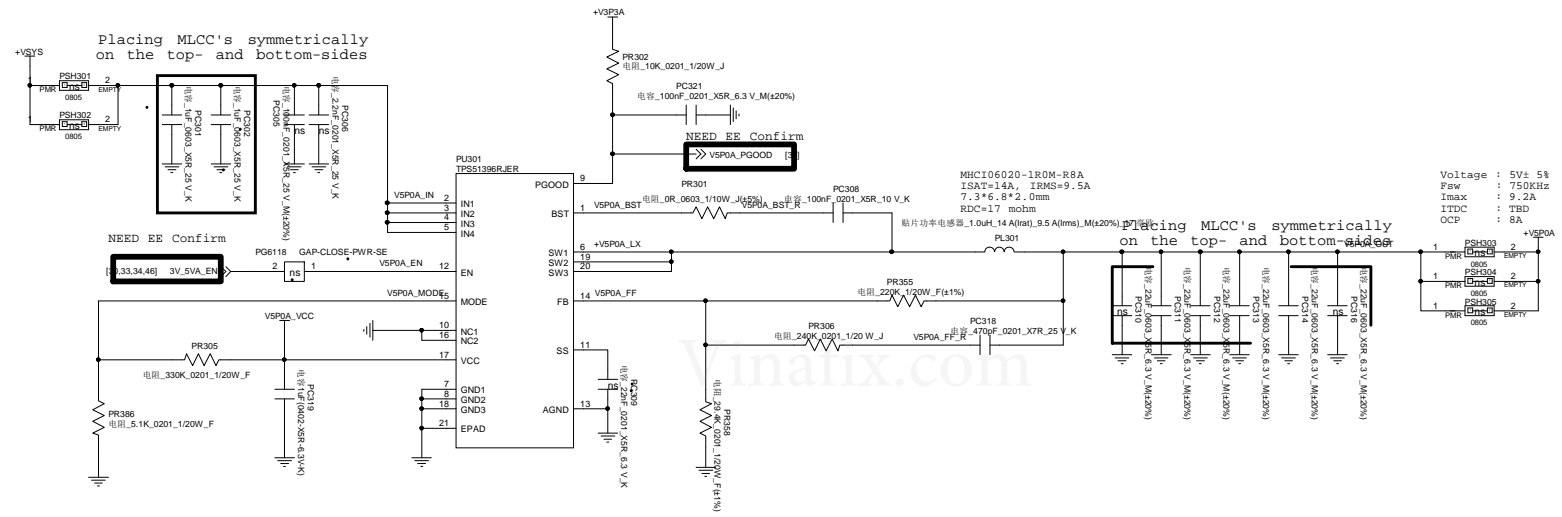
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```

Voltage : battery cell TSD
Fsw      : 800KHz
Imax     : 6.45A
ITDC     : TSD
OCP      :

```





Voltage : 5V±5%
Fsw : 750KHz
Imax : 9.2A
ITDC : TBD
OCP : 8A

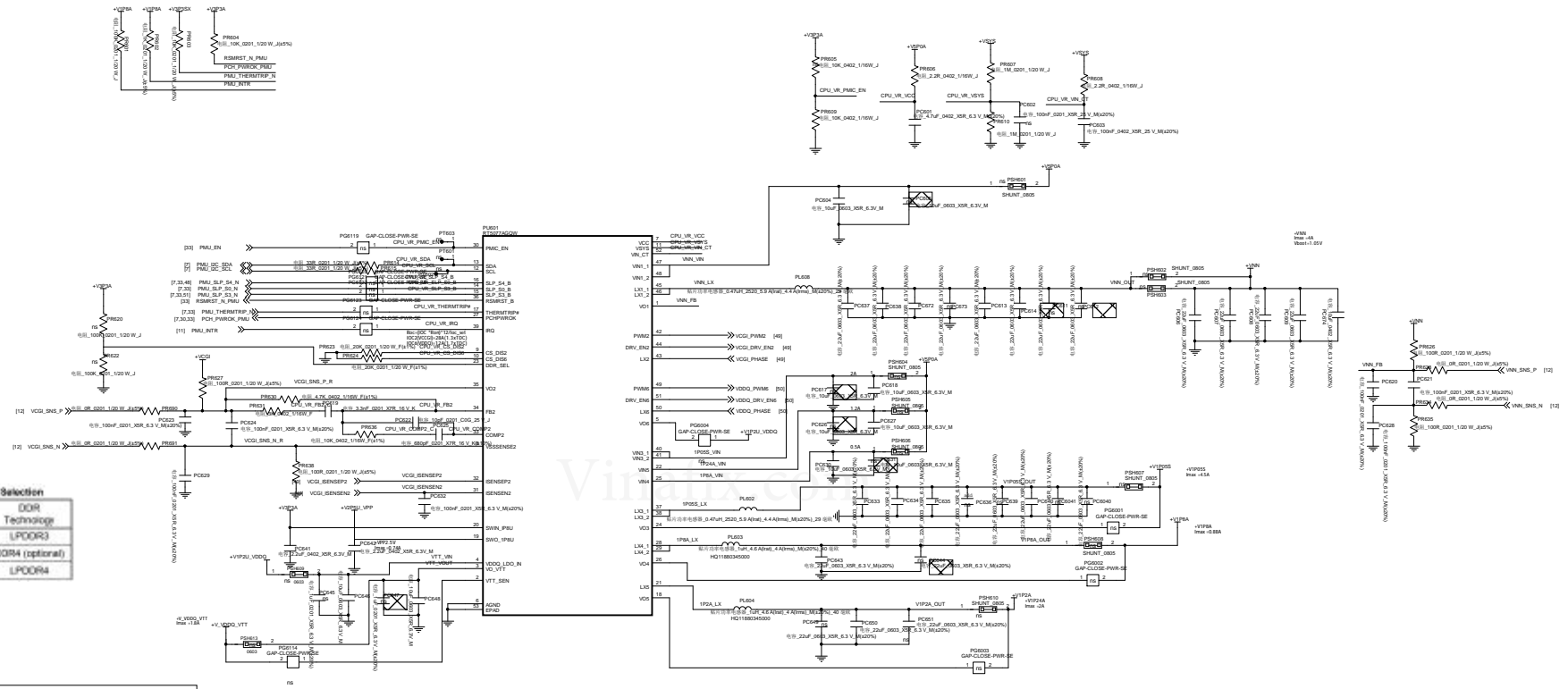
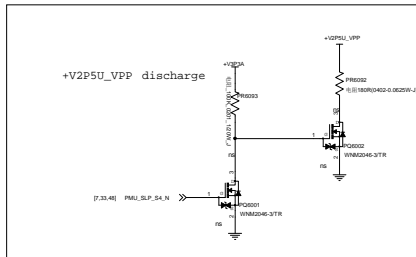
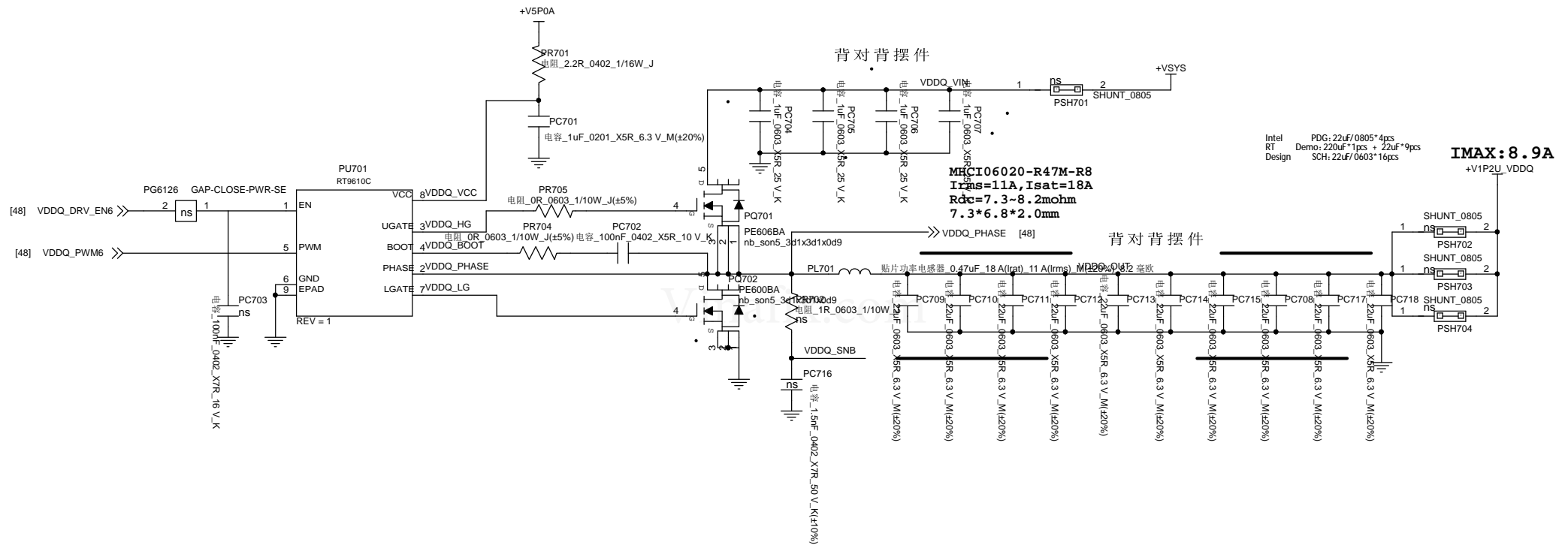


Table 2. Buck6 (DOR) Voltage Selection

DOR_SEL Pin State	Buck6 Nominal Output Voltage	DOR Technology
H	1.2V	LPDDR3
Floating	1.2V	DOR4 (optional)
L	1.1V	LPDDR4



VDDQ

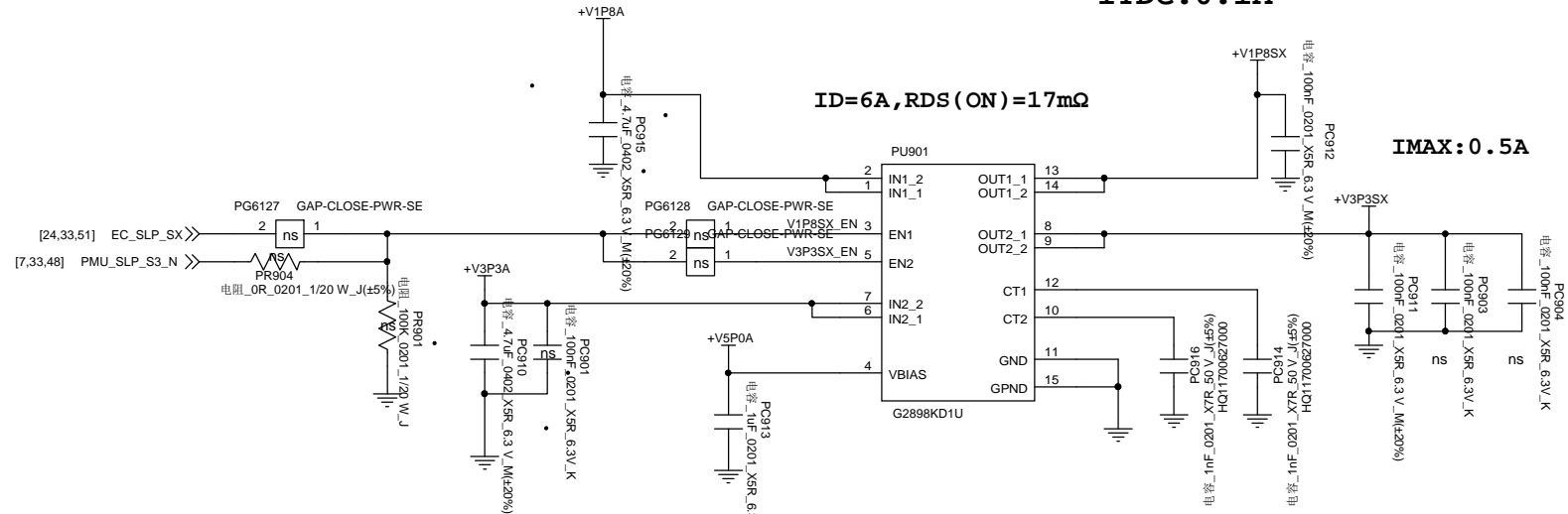


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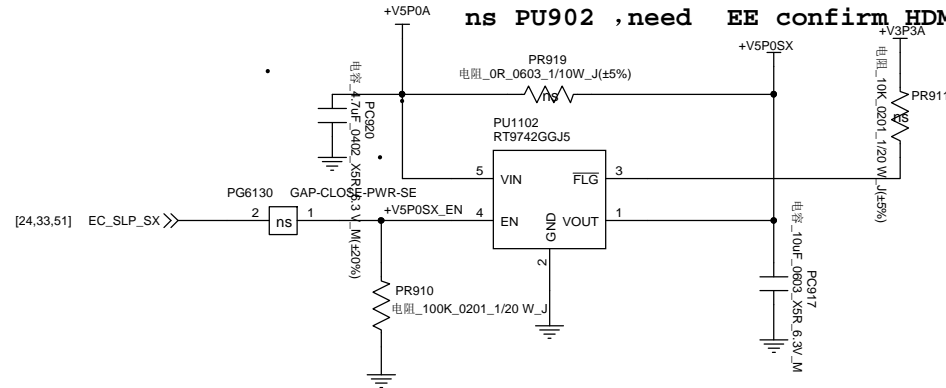
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V3P3SX V5P0SX V1P8SX

ITDC:0.1A



ns PU902 ,need EE confirm HDMI sequence




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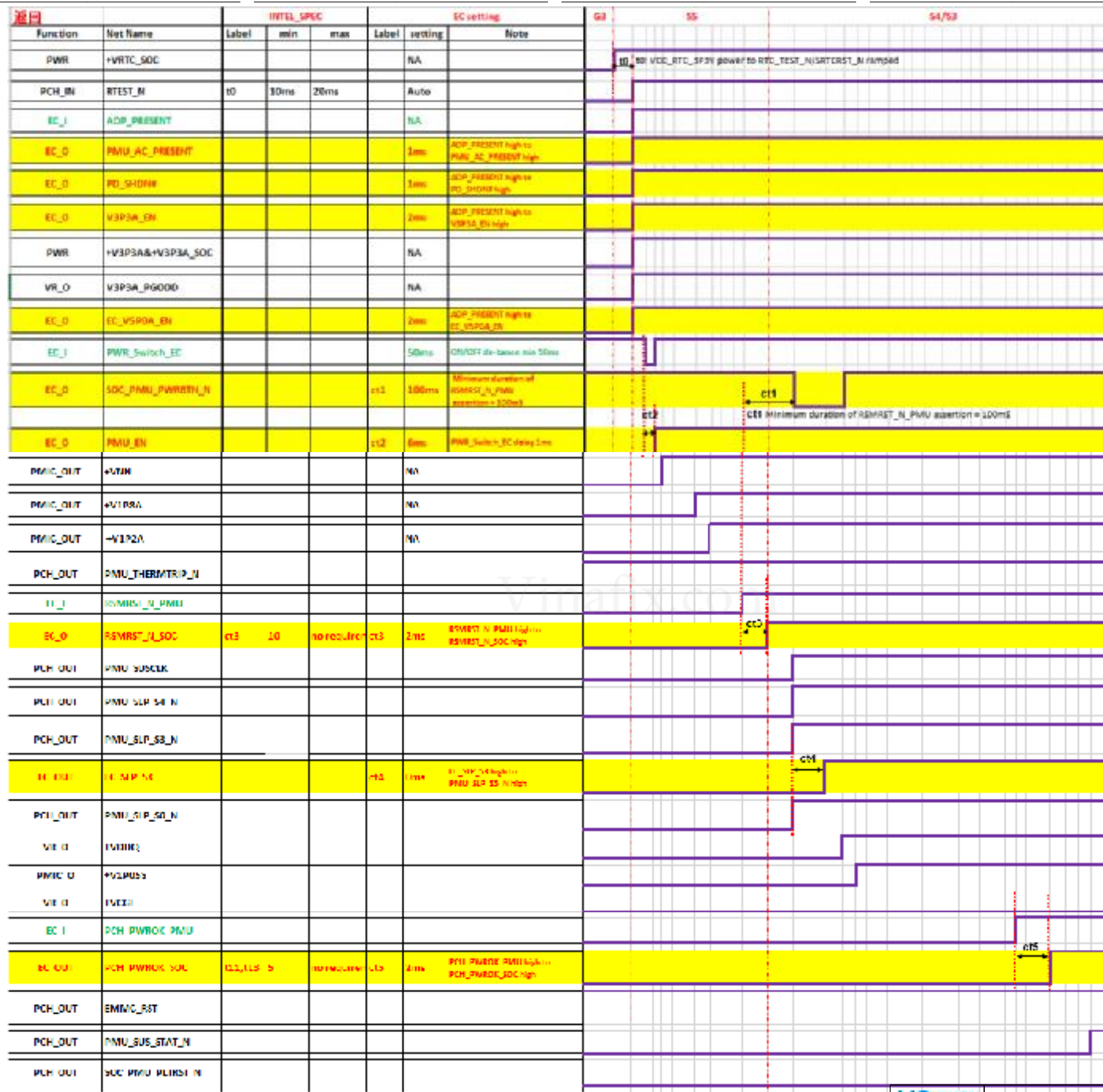
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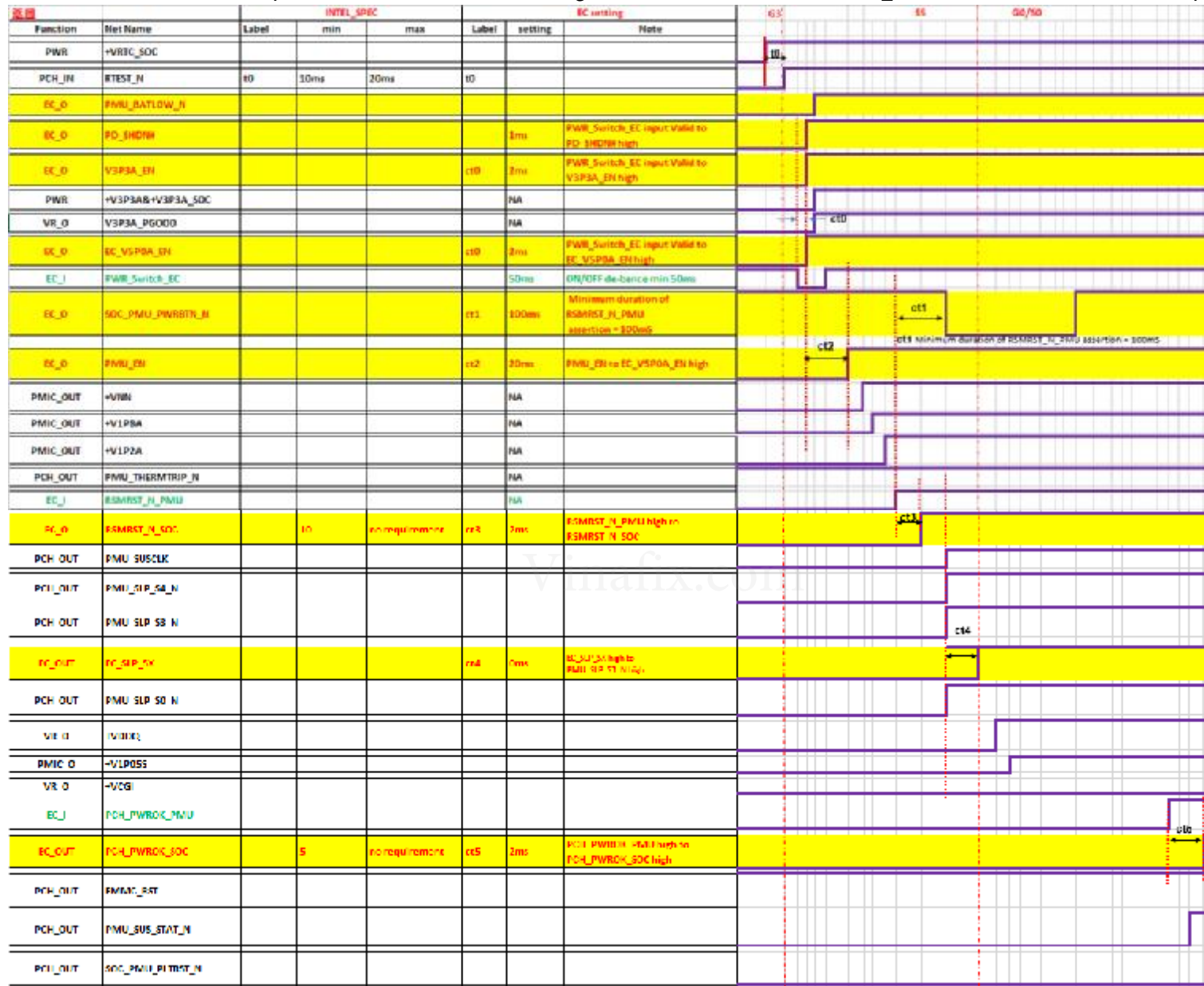
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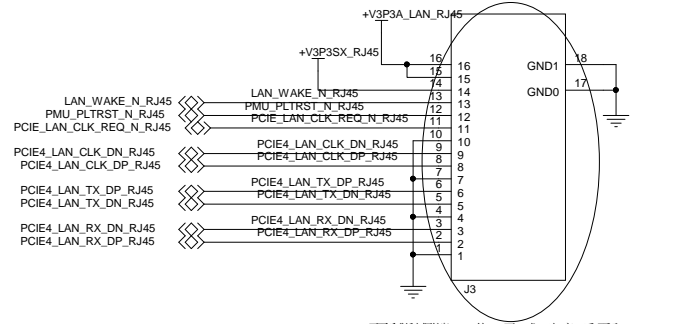
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Rev V1.0

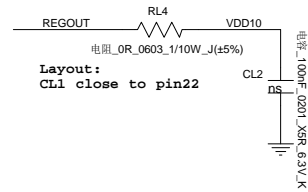
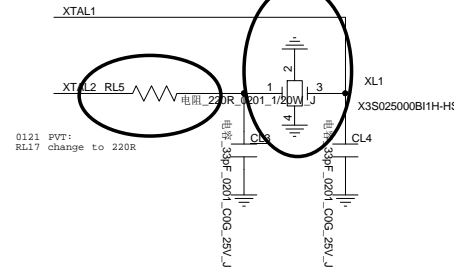
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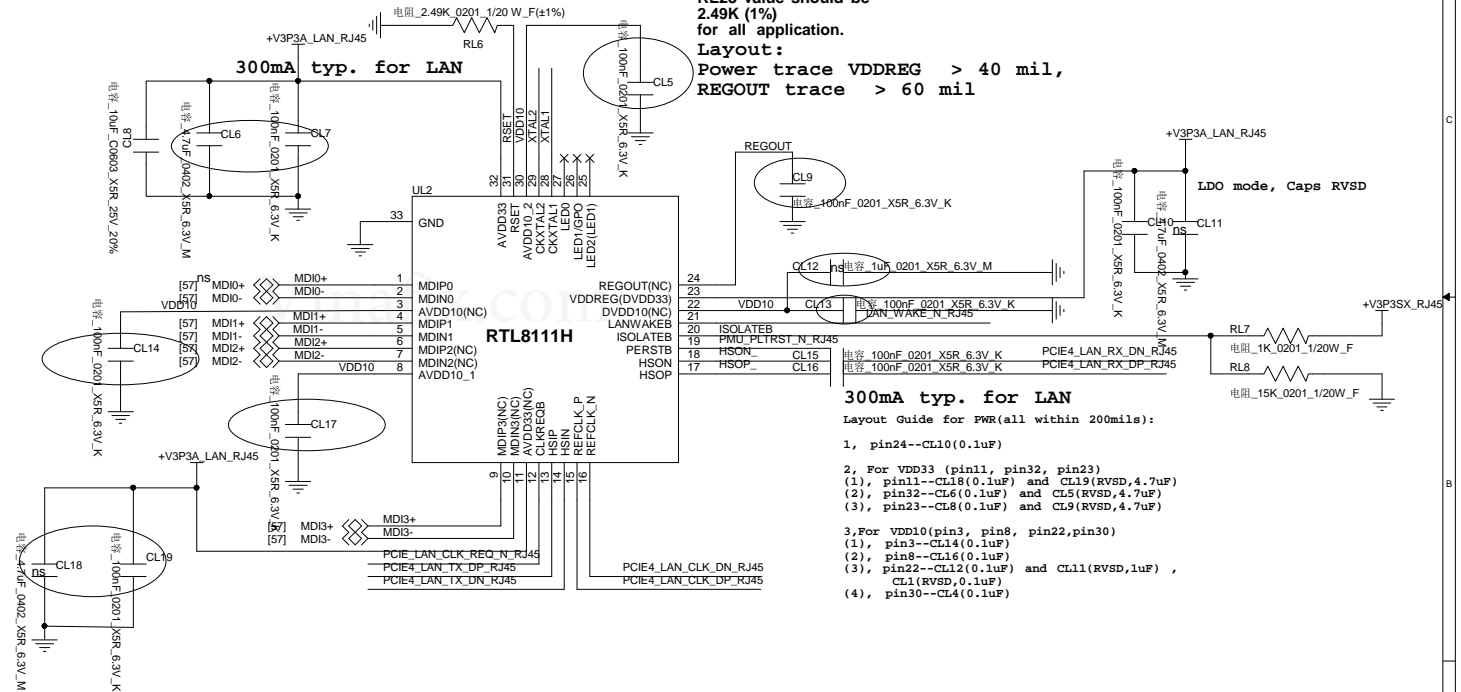


已删除器件信息，待正式建库后请修改 Say nrl.



RL23 value should be 2.49K (1%) for all application.


Layout: Power trace VDDREG > 40 mil, REGOUT trace > 60 mil



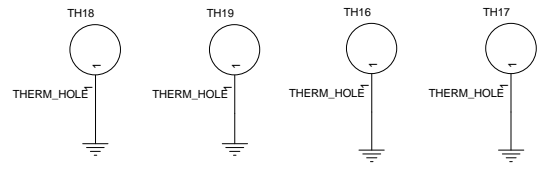
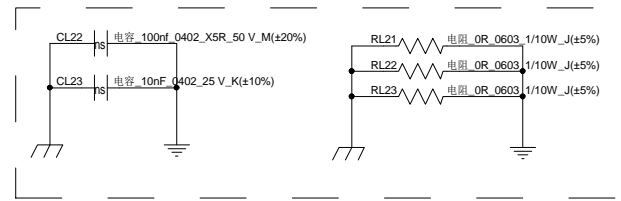
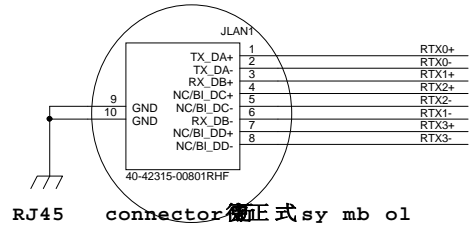
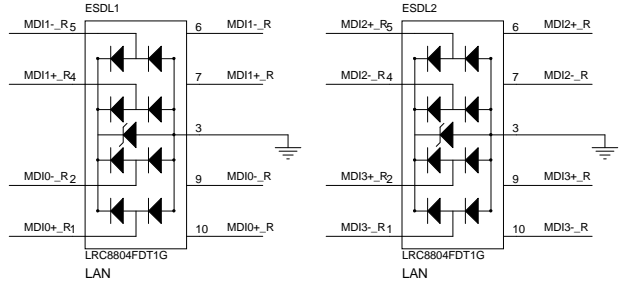
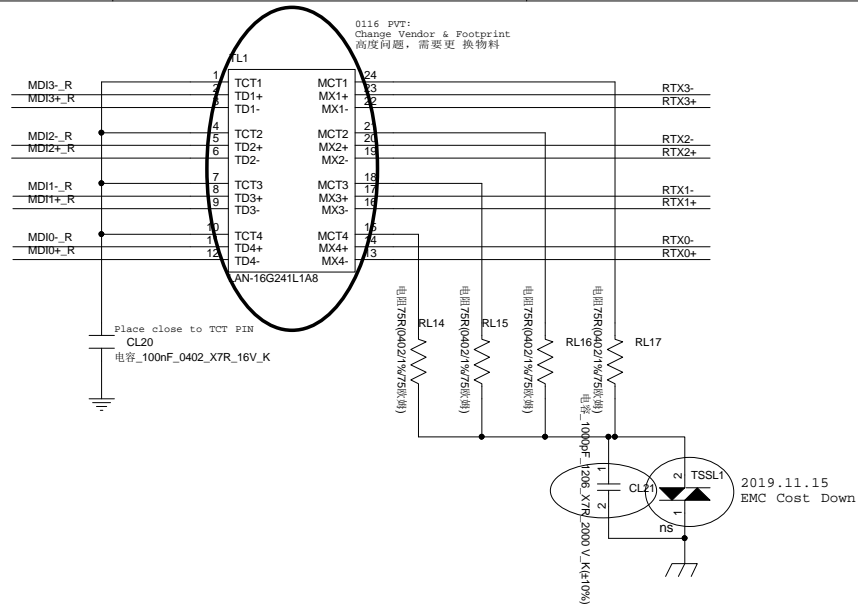
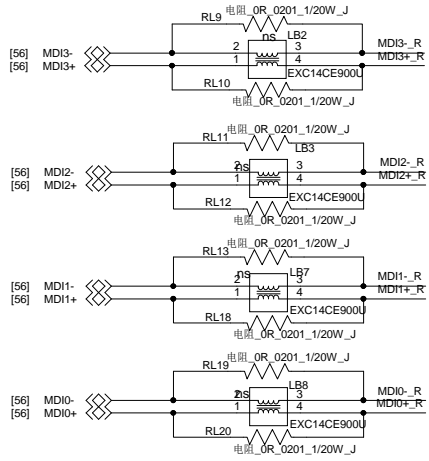
- 300mA typ. for LAN
- Layout Guide for PWR(all within 200mils):
- 1, pin24--CL10(0.1uF)
 - 2, For VDD33 (pin11, pin32, pin23)
 - (1), pin11--CL18(0.1uF) and CL19(RVSD,4.7uF)
 - (2), pin32--CL6(0.1uF) and CL5(RVSD,4.7uF)
 - (3), pin23--CL8(0.1uF) and CL9(RVSD,4.7uF)
 - 3, For VDD10 (pin3, pin8, pin22, pin30)
 - (1), pin3--CL14(0.1uF)
 - (2), pin8--CL16(0.1uF)
 - (3), pin22--CL12(0.1uF) and CL11(RVSD,1uF), CL1(RVSD,0.1uF)
 - (4), pin30--CL4(0.1uF)

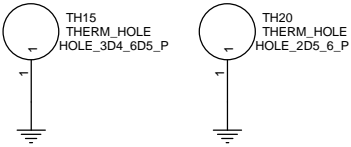
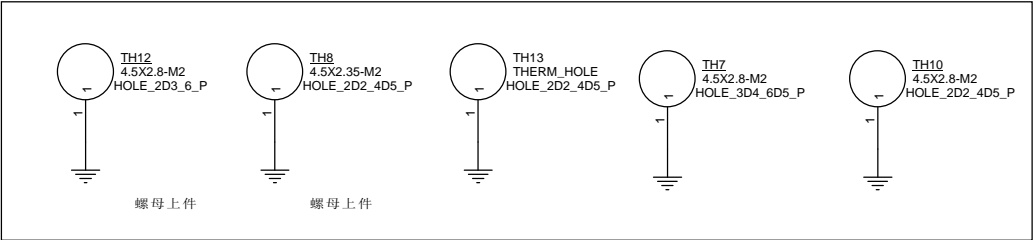
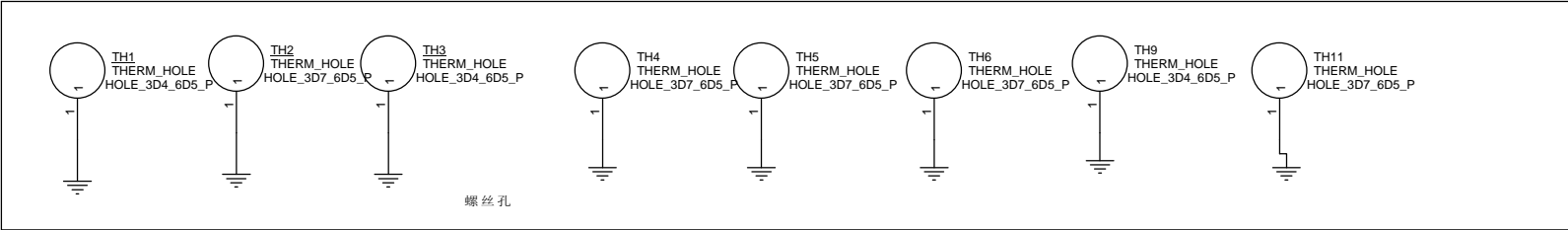
0110 PVT:
pull up power change to +3P3A

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RJ45





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<Doc>	

1.Add Battery SMBUS test point,PT603,PT604.----20180131
2.JHDD1 PIN4&PIN5 NC.----20180131
3.Memory ID table order from ID0,ID1,ID2 to ID2,ID1,ID0--20180202

4.P39 删除L4网络，增加RJ45 _ UB_CONN 2 1 5

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